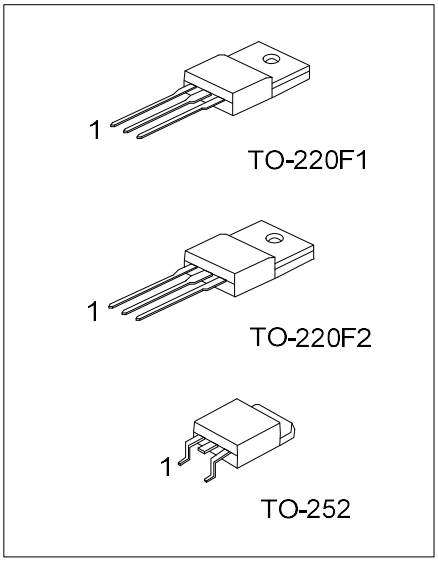
12NM95-Q **Preliminary** ***Power MOSFET***

12A, 950V N-CHANNEL SUPER-JUNCTION MOSFET



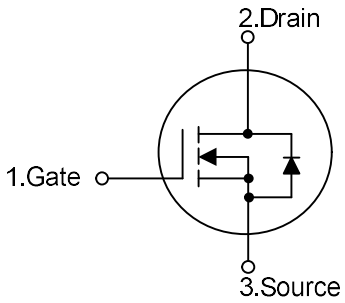
■ DESCRIPTION

The **UTC 12NM95-Q** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

■ FEATURES

* $R_{DS(ON)} \leq 0.75\ \Omega$ @ V_{GS} = 10V, I_D = 4.5A
* Fast switching capability
* Avalanche energy tested
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
12NM95L-Q-TF1-T	12NM95G-Q-TF1-T	TO-220F1	G	D	S	Tube
12NM95L-Q-TF2-T	12NM95G-Q-TF2-T	TO-220F2	G	D	S	Tube
12NM95L-Q-TN3-R	12NM95G-Q-TN3-R	TO-252	G	D	S	Tape Reel

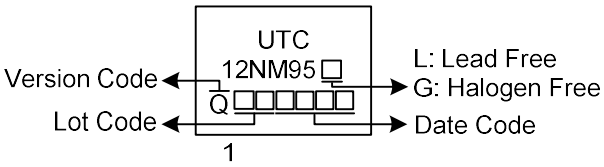
Note: Pin Assignment: G: Gate D: Drain S: Source

12NM95G-Q-TF1-T

(1)Packing Type	(1) T: Tube, R: Tape Reel
(2)Package Type	(2) TF1: TO-220F1, TF2: TO-220F2, TN3: TO-252
(3)Version Code	(3) Version Q
(4)Green Package	(4) G: Halogen Free and Lead Free, L: Lead Free

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■ MARKING


UTC
12NM95 □
Q □□□□□□
Version Code
Lot Code
1
L: Lead Free
G: Halogen Free
Date Code

■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified.)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V_{DSS}	950	V
Gate-Source Voltage			V_{GSS}	±30	V
Drain Current	Continuous	T_C=25°C	I_D	12	A
		T_C=100°C		7.8	A
	Pulsed (Note 2)		I_{DM}	36	A
Avalanche Energy	Single Pulsed (Note 3)		E_{AS}	420	mJ
MOSFET dv/dt Ruggedness			dv/dt	50	V/ns
Peak Diode Recovery dv/dt (Note 4)				1.3	V/ns
Power Dissipation		TO-220F1 TO-220F2	P_D	22	W
		TO-252		37	W
Junction Temperature			T_J	+150	°C
Storage Temperature			T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L = 100mH, I_{AS} = 2.9A, V_{DD} = 90V, R_G = 25Ω, Starting T_J = 25°C.
4. I_{SD} ≤ 12A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220F1 TO-220F2	θ_{JA}	62.5	°C/W
	TO-252		110	°C/W
Junction to Case	TO-220F1 TO-220F2	θ_{JC}	5.68	°C/W
	TO-252		3.37 (Note)	°C/W

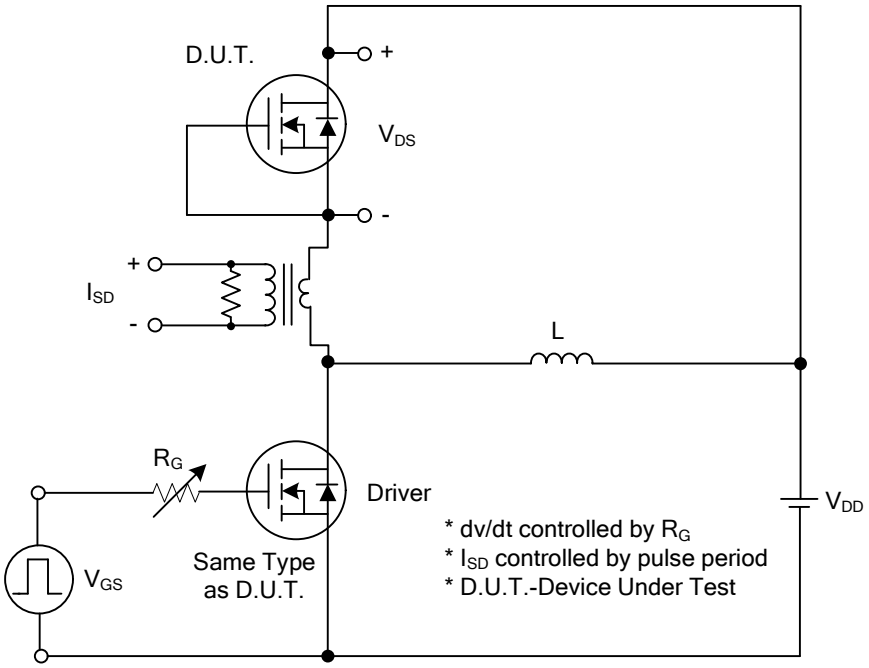
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified.)

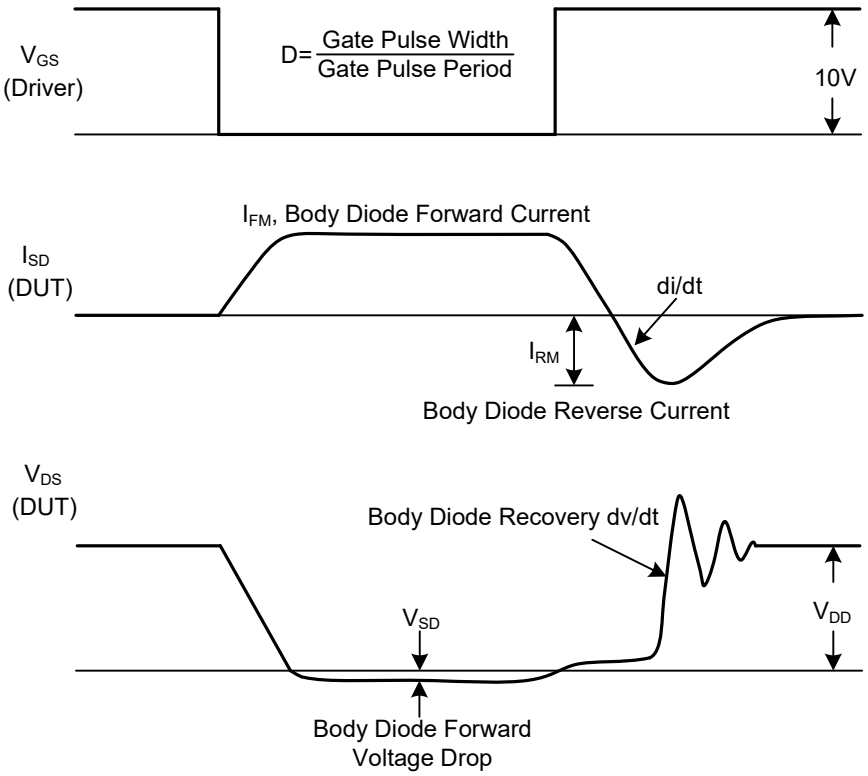
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	950			V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=950V, V_{GS}=0V			10	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.5		4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=4.5A		0.67	0.75	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=50V, f=1MHz		910		pF
Output Capacitance	C_{OSS}			120		pF
Reverse Transfer Capacitance	C_{RSS}			2.2		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q_G	V_{DS}=720V, V_{GS}=10V, I_D=12A (Note 1, 2)		48		nC
Gate-Source Charge	Q_{GS}			13		nC
Gate-Drain Charge	Q_{DD}			19		nC
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=100V, V_{GS}=10V, I_D=12A, R_G =25Ω (Note 1, 2)		12		ns
Turn-On Rise Time	t_R			24		ns
Turn-Off Delay Time	$t_{D(OFF)}$			102		ns
Turn-Off Fall Time	t_F			44		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				12	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				36	A
Drain-Source Diode Forward Voltage	V_{SD}	I_S=12A, V_{GS}=0V			1.4	V
Body Diode Reverse Recovery Time	t_{rr}	I_S=12A, V_{GS}=0V, dI_F/dt=100A/μs		530		nS
Body Diode Reverse Recovery Charge	Q_{rr}			9		μC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

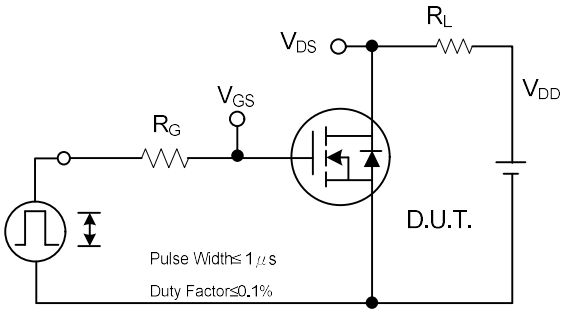


Peak Diode Recovery dv/dt Test Circuit

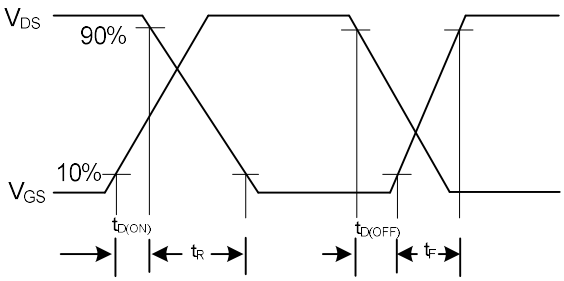


Peak Diode Recovery dv/dt Waveforms

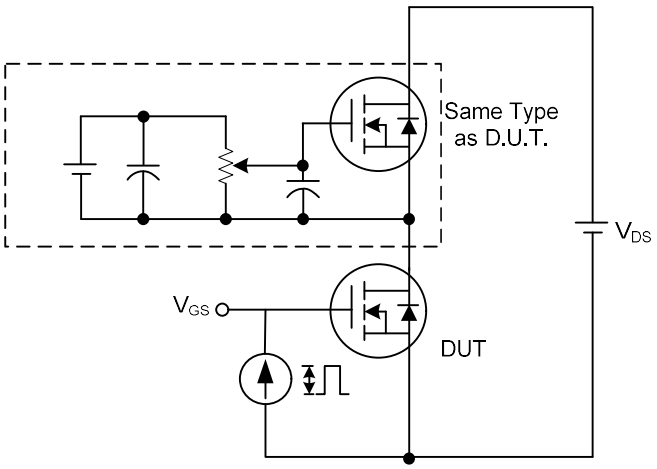
■ TEST CIRCUITS AND WAVEFORMS



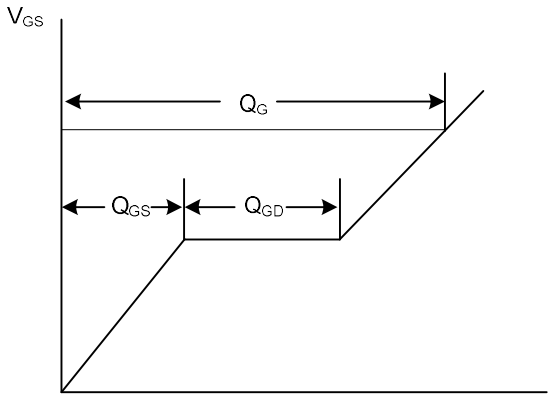
Switching Test Circuit



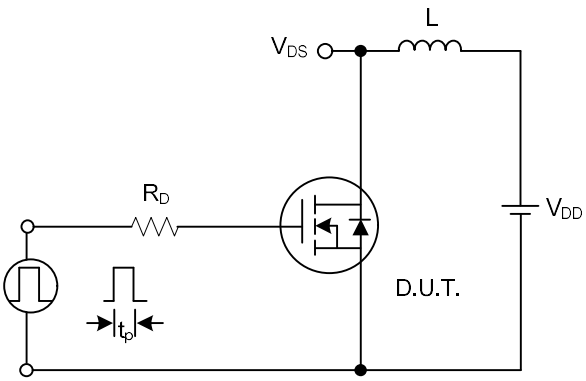
Switching Waveforms



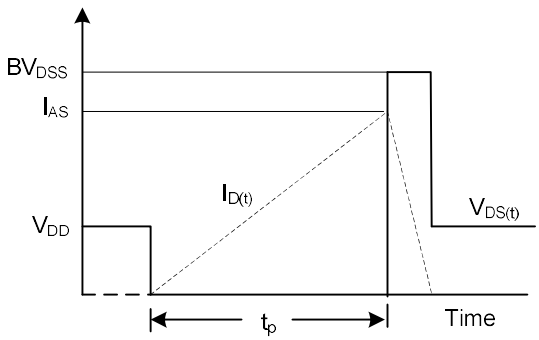
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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