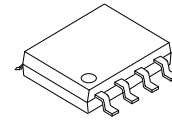


**15NN10M***Power MOSFET***15A, 100V DUAL N-CHANNEL
ENHANCEMENT MODE POWER
MOSFET****DESCRIPTION**

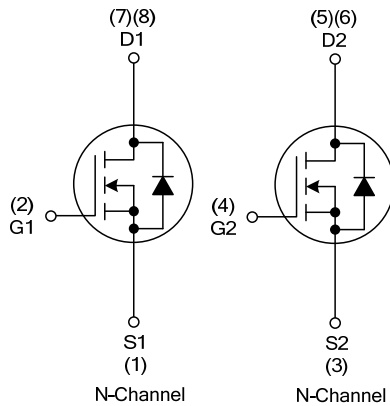
The UTC **15NN10M** is a Dual N-channel enhancement mode power MOSFET using UTC's perfect technology to provide customers with fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

FEATURES

- * $R_{DS(ON)} \leq 90 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=7.5\text{A}$
- * $R_{DS(ON)} \leq 100 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=7.5\text{A}$
- * High switching speed
- * Low Gate Charge
- * Simple Drive Requirement



SOP-8

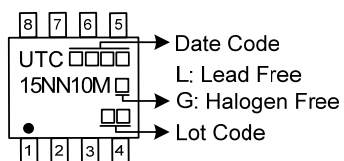
SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment							Packing
Lead Free	Halogen Free		1	2	3	4	5, 6	7, 8		
15NN10ML-S08-R	15NN10MG-S08-R	SOP-8	S1	G1	S2	G2	D2	D1	Tape Reel	

Note: Pin Assignment: G: Gate D: Drain S: Source

15NN10MG-S08-R	(1) Packing Type	(1) R: Tape Reel
	(2) Package Type	(2) S08: SOP-8
	(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ **ABSOLUTE MAXIMUM RATING** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	DC	I_D	15	A
	Pulsed (Note 2)	I_{DM}	30	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	31.2	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	5	V/ns
Power Dissipation		P_D	4.2	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
 3. $L = 0.1\text{mH}$, $I_{AS} = 25\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$.
 4. $I_{SD} \leq 15\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^{\circ}\text{C}$.

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	125	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	29.7	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

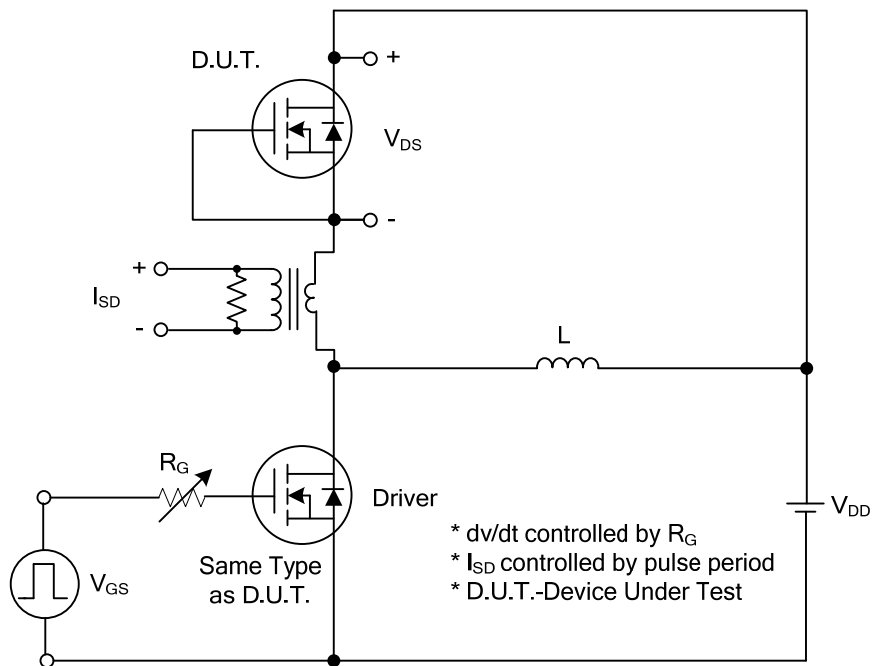
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	100			V
Drain-Source Leakage Current		I _{DSS}	V _D =100V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _D =0V			+100	nA
	Reverse		V _{GS} =-20V, V _D =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _D =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =7.5A			90	mΩ
			V _{GS} =4.5V, I _D =7.5A			100	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _D =25V, f=1.0MHz		751		pF
Output Capacitance		C _{OSS}			114		pF
Reverse Transfer Capacitance		C _{RSS}			17		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _D =80V, V _{GS} =10V, I _D =15A (Note 1, 2)		25		nC
Gate to Source Charge		Q _{GS}			6		nC
Gate to Drain Charge		Q _{GD}			12		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =50V, V _{GS} =10V, I _D =15A, R _G =25Ω (Note 1, 2)		8		ns
Rise Time		t _R			17		ns
Turn-OFF Delay Time		t _{D(OFF)}			70		ns
Fall-Time		t _F			22		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				15	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				30	A
Diode Forward Voltage		V _{SD}	I _F =15A, V _{GS} =0V			1.4	V
Reverse Recovery Time		t _{rr}	I _S =15A, V _{GS} =0V,		105		ns
Reverse Recovery Charge (Note 1)		Q _{rr}	di _F /dt = 100 A/μs		260		nC

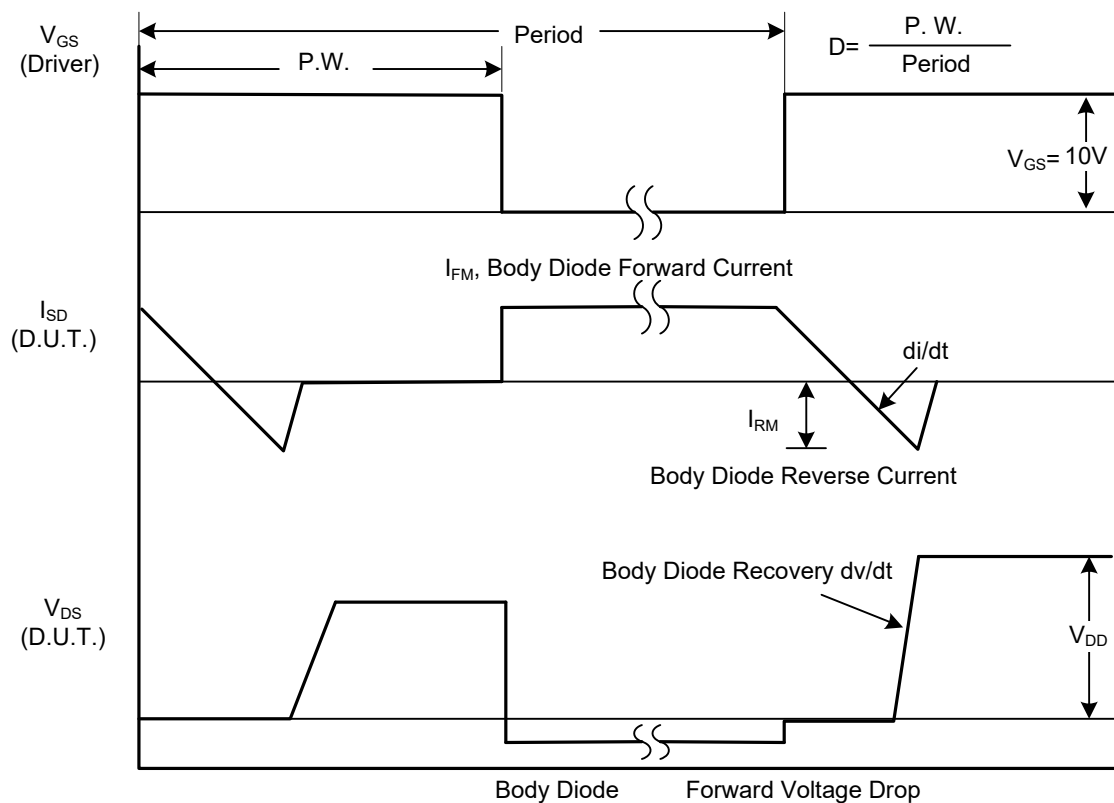
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

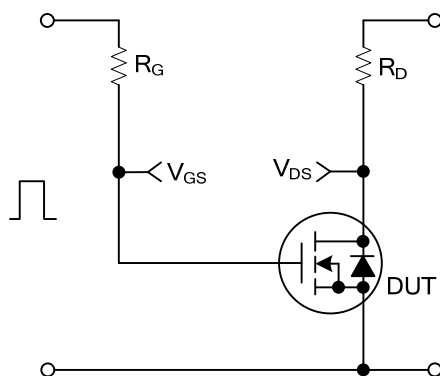


Peak Diode Recovery dv/dt Test Circuit

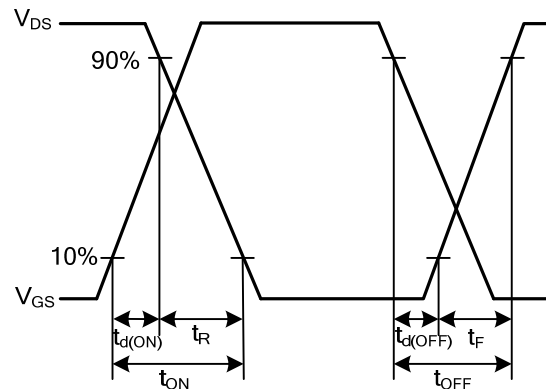


Peak Diode Recovery dv/dt Waveforms

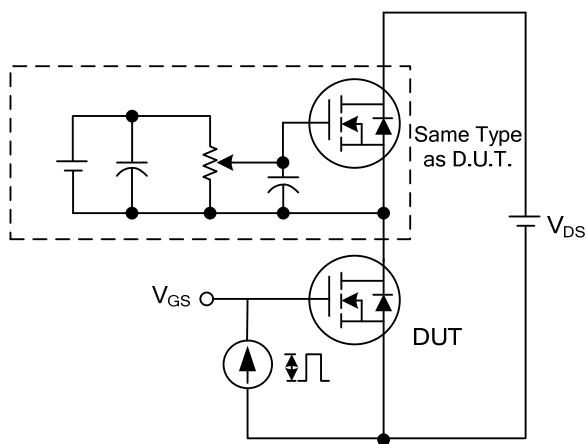
■ TEST CIRCUITS AND WAVEFORMS



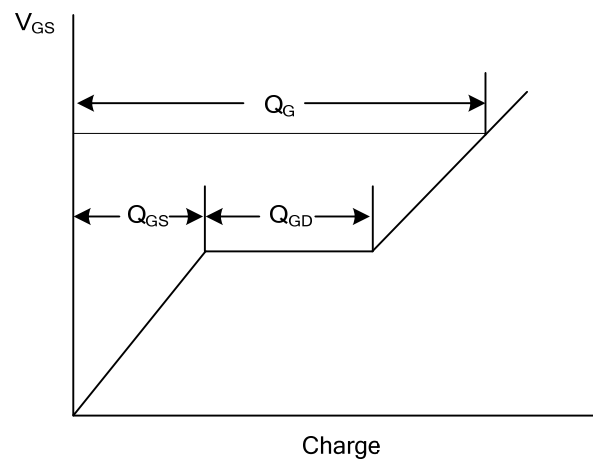
Switching Test Circuit



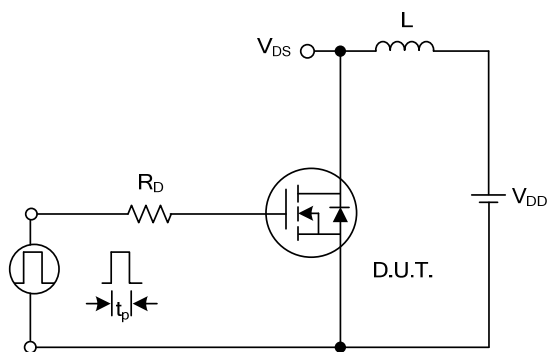
Switching Waveforms



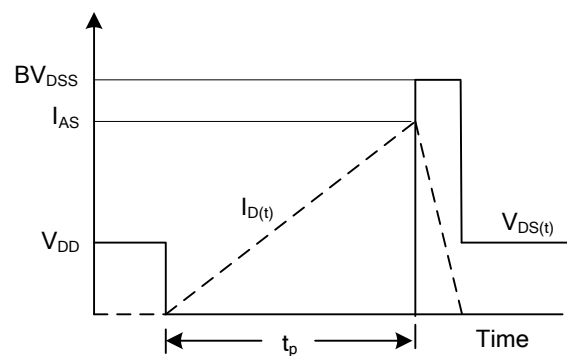
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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