

**18NM100Z**

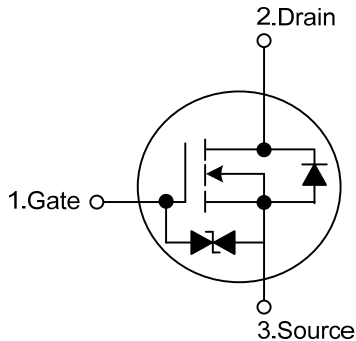
Preliminary

POWER MOSFET**18A, 1000V N-CHANNEL
SUPER-JUNCTION MOSFET****DESCRIPTION**

The UTC **18NM100Z** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

FEATURES

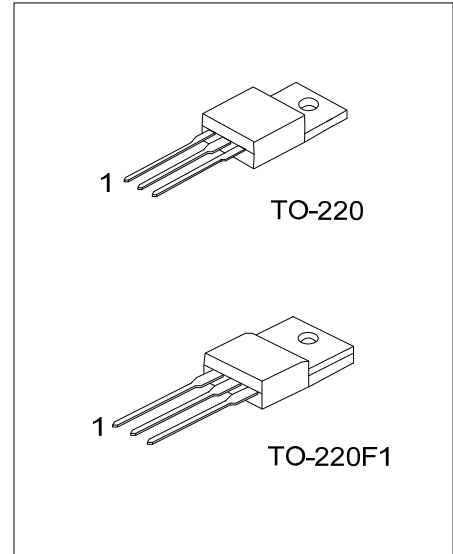
- * $R_{DS(ON)} \leq 0.45 \Omega$ @ $V_{GS}=10V$, $I_D=9.0A$
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness
- * With ESD protection

SYMBOL**ORDERING INFORMATION**

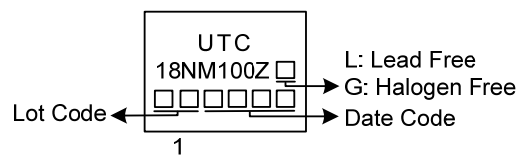
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
18NM100ZL-TA3-T	18NM100ZG-TA3-T	TO-220	G	D	S	Tube
18NM100ZL-TF1-T	18NM100ZG-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

18NM100ZG-TA3-T	(1)Packing Type	(1) T: Tube
	(2)Package Type	(2) TA3: TO-220, TF1: TO-220F1
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



■ MARKING



■ **ABSOLUTE MAXIMUM RATING** ($T_C=25^{\circ}\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	1000	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	DC	I_D	18	A
	Pulsed (Note 2)	I_{DM}	54	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	276	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.3	V/ns
Power Dissipation	TO-220	P_D	125	W
	TO-220F1		34	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 100\text{mH}$, $I_{AS} = 2.35\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$.

4. $I_{SD} \leq 18\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$.

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-220	θ_{JC}	1	$^{\circ}\text{C}/\text{W}$
	TO-220F1		3.6	$^{\circ}\text{C}/\text{W}$

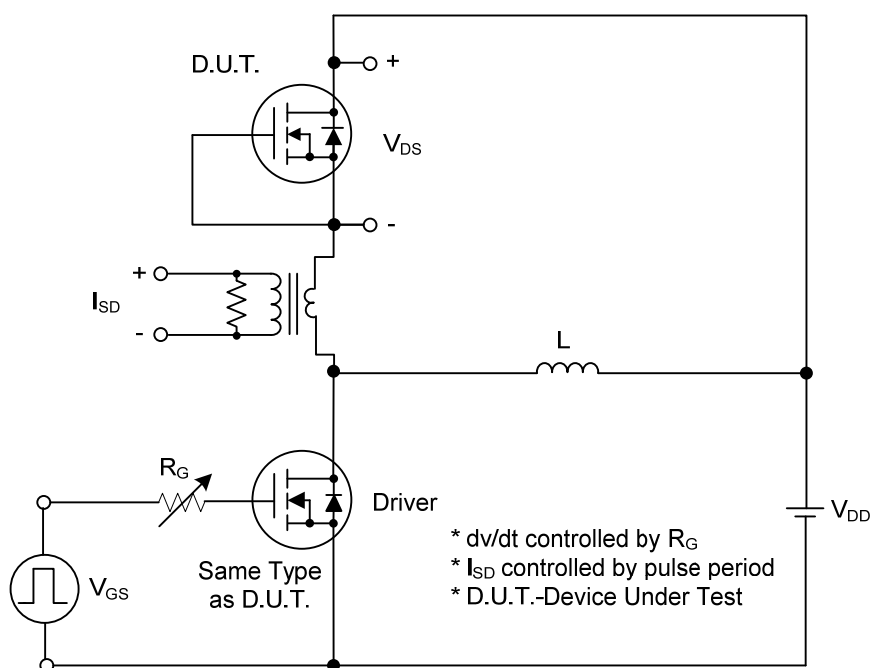
■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	1000			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =1000V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+10	μA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-10	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.5		4.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =9.0A			0.45	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =50V, f=1.0MHz		1533		pF
Output Capacitance		C _{OSS}			93		pF
Reverse Transfer Capacitance		C _{RSS}			3		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =800V, V _{GS} =10V, I _D =18A (Note 1, 2)		72		nC
Gate to Source Charge		Q _{GS}			17		nC
Gate to Drain Charge		Q _{GD}			25		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =18A, R _G =25Ω (Note 1, 2)		22		ns
Rise Time		t _R			29		ns
Turn-OFF Delay Time		t _{D(OFF)}			217		ns
Fall-Time		t _F			75		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				18	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				54	A
Diode Forward Voltage		V _{SD}	I _F =18A, V _{GS} =0V			1.4	V
Reverse Recovery Time		t _{rr}	I _S =18A, V _{GS} =0V,		500		ns
Reverse Recovery Charge (Note 1)		Q _{rr}	dI _F /dt = 100 A/μs		13		μC

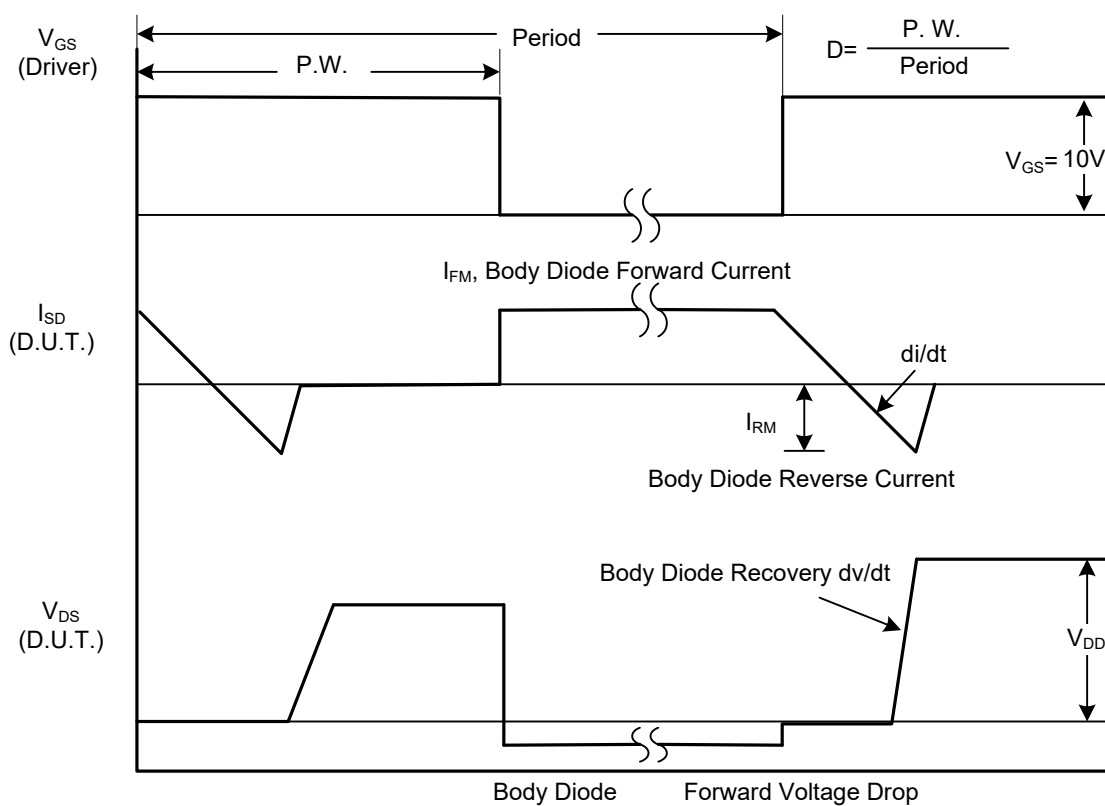
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

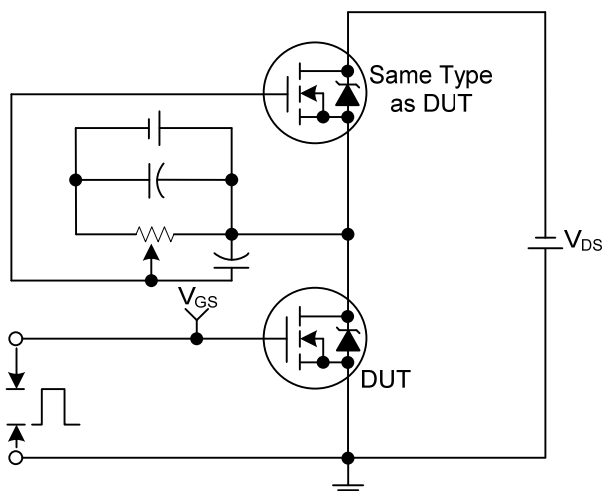


Peak Diode Recovery dv/dt Test Circuit

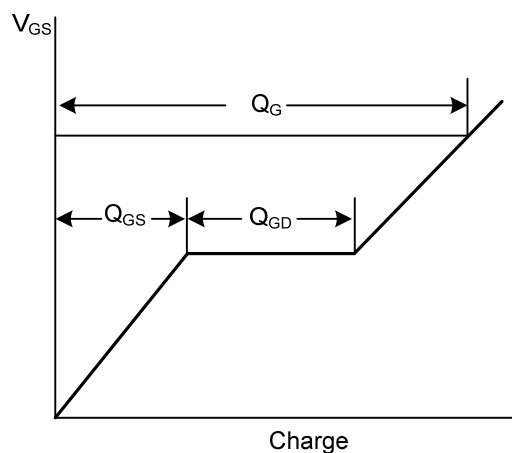


Peak Diode Recovery dv/dt Waveforms

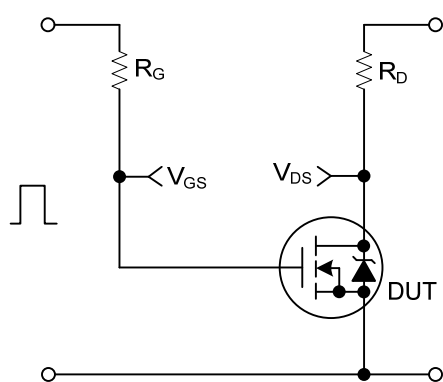
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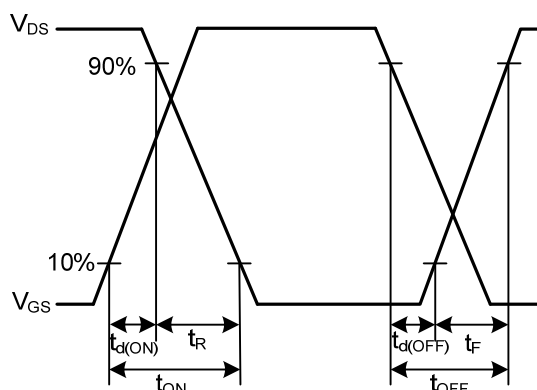
Gate Charge Test Circuit



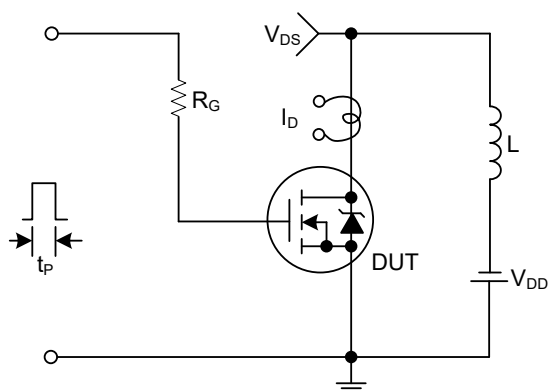
Gate Charge Waveforms



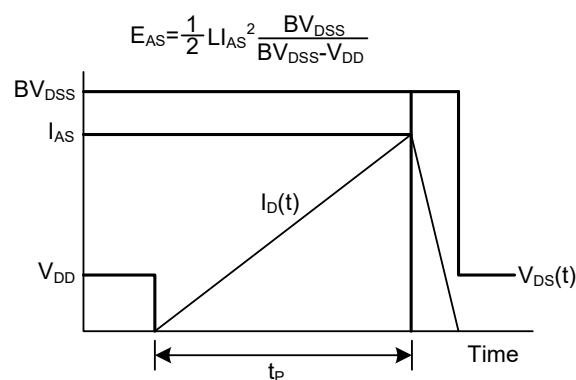
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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