



2NM65-VQ

Preliminary

Power MOSFET

2.0A, 650V N-CHANNEL SUPER-JUNCTION MOSFET

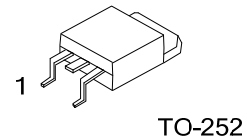
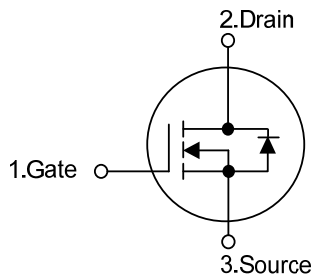
DESCRIPTION

The **UTC 2NM65-VQ** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

FEATURES

- * $R_{DS(ON)} \leq 3.8 \Omega$ @ $V_{GS}=10V$, $I_D=1.0A$
 $R_{DS(ON)} \leq 4.2 \Omega$ @ $V_{GS}=4.5V$, $I_D=1.0A$
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

SYMBOL



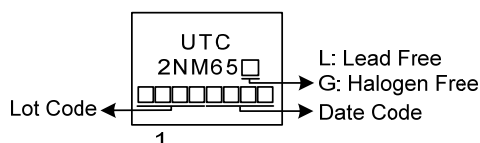
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2NM65L-TN3-R	2NM65G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

	(1) Packing Type	(1) R: Tape Reel
	(2) Package Type	(2) TN3: TO-252
	(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 30	V
Drain Current	Continuous	I_D	2	A
	Pulsed (Note 2)	I_{DM}	4	A
Avalanche Energy (Note 3)	Single Pulsed	E_{AS}	42	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.1	V/ns
Power Dissipation		P_D	18	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 100\text{mH}$, $I_{AS} = 0.92\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$ Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 2.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	6.94 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

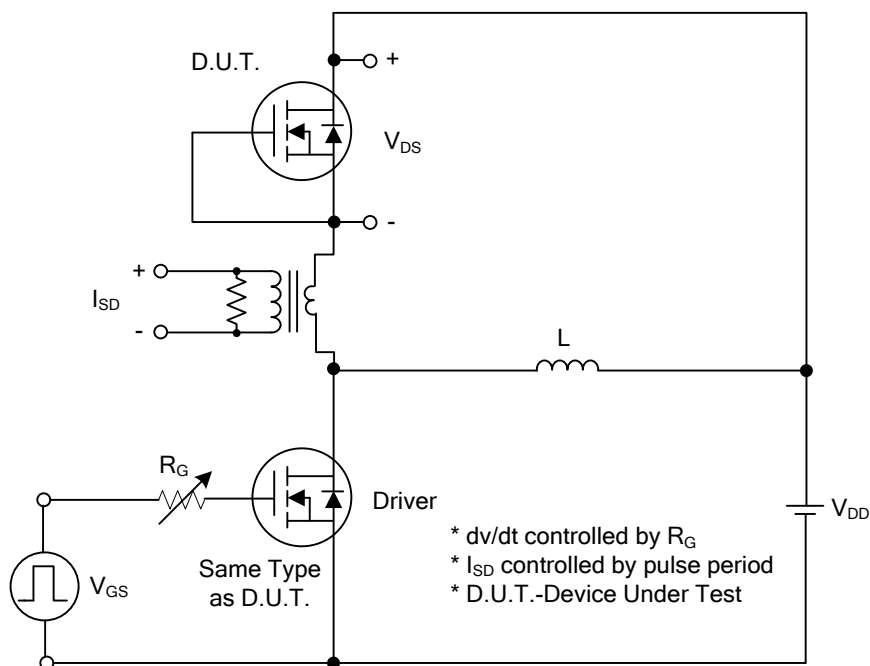
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	650			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =650V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =30V, V _{DS} =0V			100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =1.0A			3.8	Ω
			V _{GS} =4.5V, I _D =1.0A			4.2	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =50V, f=1MHz		138		pF
Output Capacitance		C _{OSS}			19		pF
Reverse Transfer Capacitance		C _{RSS}			2.2		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =520V, V _{GS} =10V, I _D =0.5A (Note 1, 2)		14		nC
Gate-Source Charge		Q _{GS}			3		nC
Gate-Drain Charge		Q _{GD}			2.8		nC
Turn-On Delay Time (Note 1)		t _{D(ON)}	V _{DS} =100V, V _{GS} =10V, I _D =0.5A, R _G =25Ω (Note 1, 2)		2.4		ns
Turn-On Rise Time		t _R			17.7		ns
Turn-Off Delay Time		t _{D(OFF)}			17.6		ns
Turn-Off Fall Time		t _F			24		ns
DRAIN-SOURCE DIODE CHARACTERISTICS							
Continuous Drain-Source Current		I _S				2	A
Maximum Body-Diode Pulsed Current		I _{SM}				4	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =2.0A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)		t _{rr}	I _S =2.0A, V _{GS} =0V		244		nS
Body Diode Reverse Recovery Charge		Q _{rr}	dI/dt=100A/μs		0.8		μC

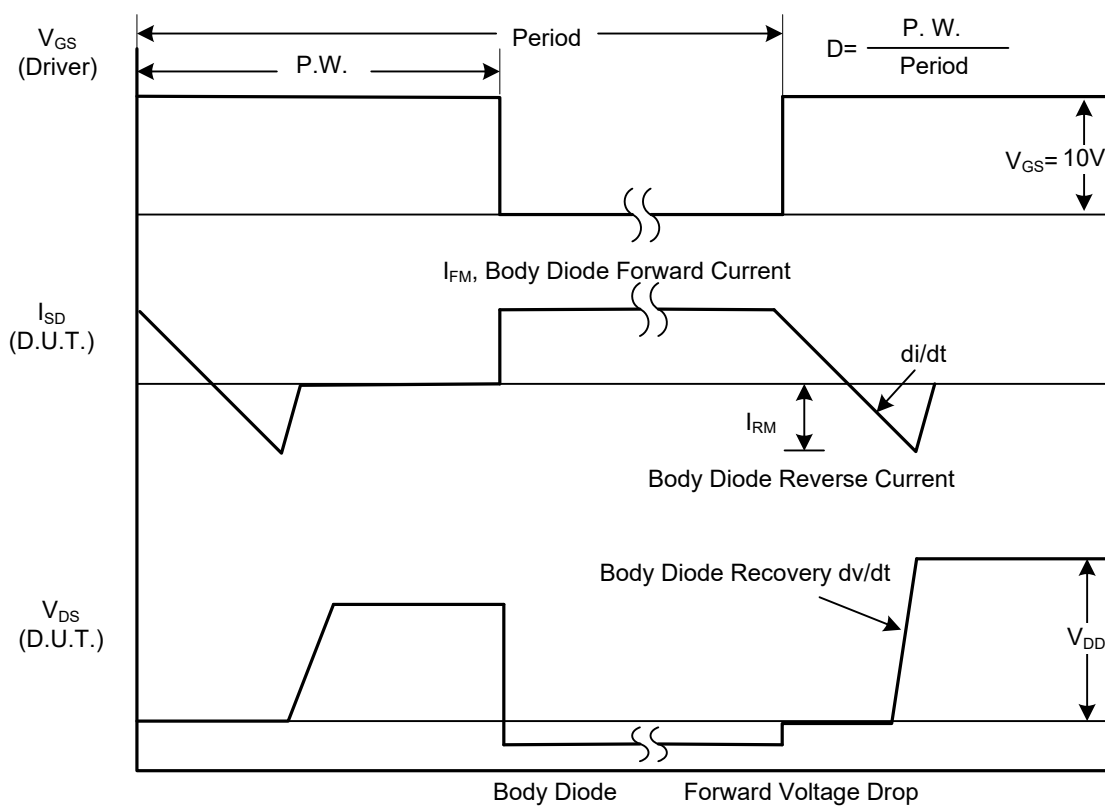
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

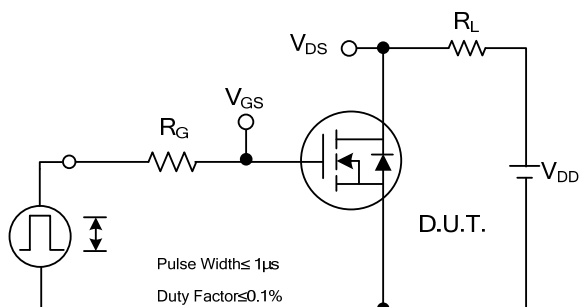


Peak Diode Recovery dv/dt Test Circuit

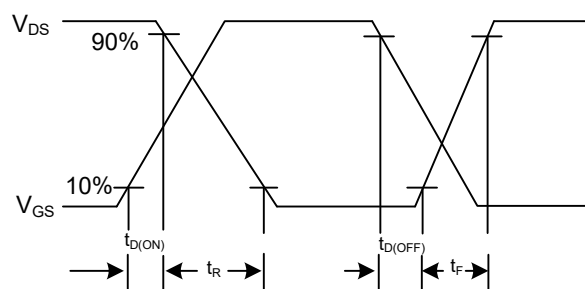


Peak Diode Recovery dv/dt Waveforms

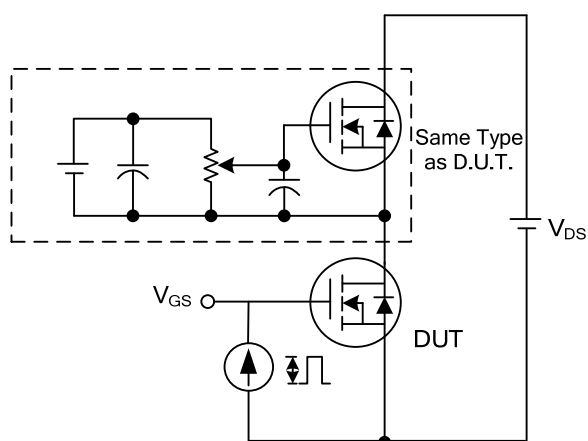
■ TEST CIRCUITS AND WAVEFORMS



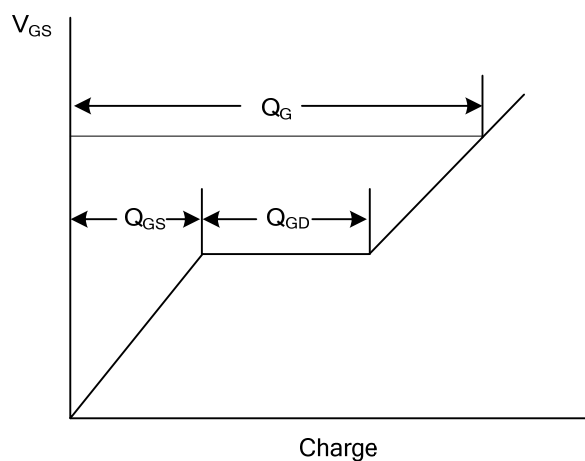
Switching Test Circuit



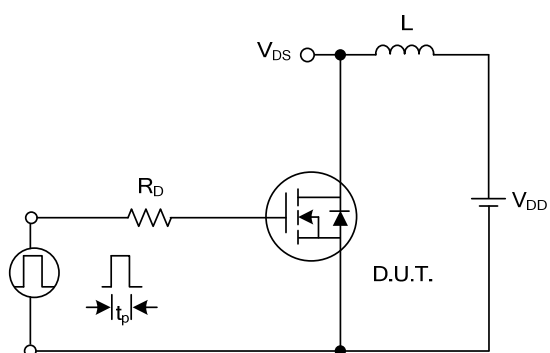
Switching Waveforms



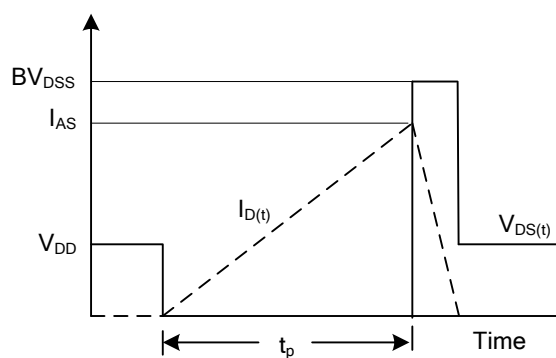
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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