

**5N60-ML1**

Preliminary

*Power MOSFET***5.0A, 600V N-CHANNEL
POWER MOSFET****DESCRIPTION**

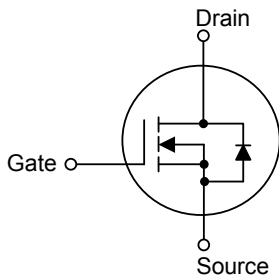
The UTC **5N60-ML1** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **5N60-ML1** is generally applied in high efficiency switch mode power supplies.

FEATURES

* $R_{DS(ON)} \leq 2.5 \Omega$ @ $V_{GS}=10V$, $I_D=2.5A$

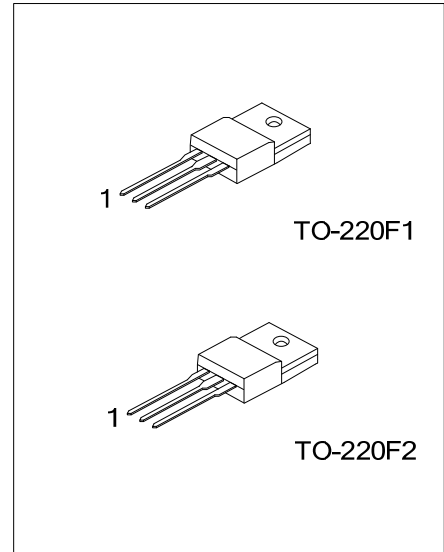
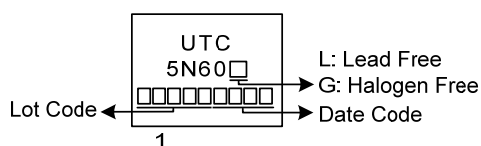
* High Switching Speed

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
5N60L-TF1-T	5N60G-TF1-T	TO-220F1	G	D	S	Tube
5N60L-TF2-T	5N60G-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

(1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube (2) TF1: TO-220F1, TF2: TO-220F2 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	600	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	5	A
	Pulsed (Note 2)	I_{DM}	10	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	172.8	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.6	V/ns
Power Dissipation		P_D	32	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 30\text{mH}$, $I_{AS} = 3.3\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$ Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 5.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	3.9	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

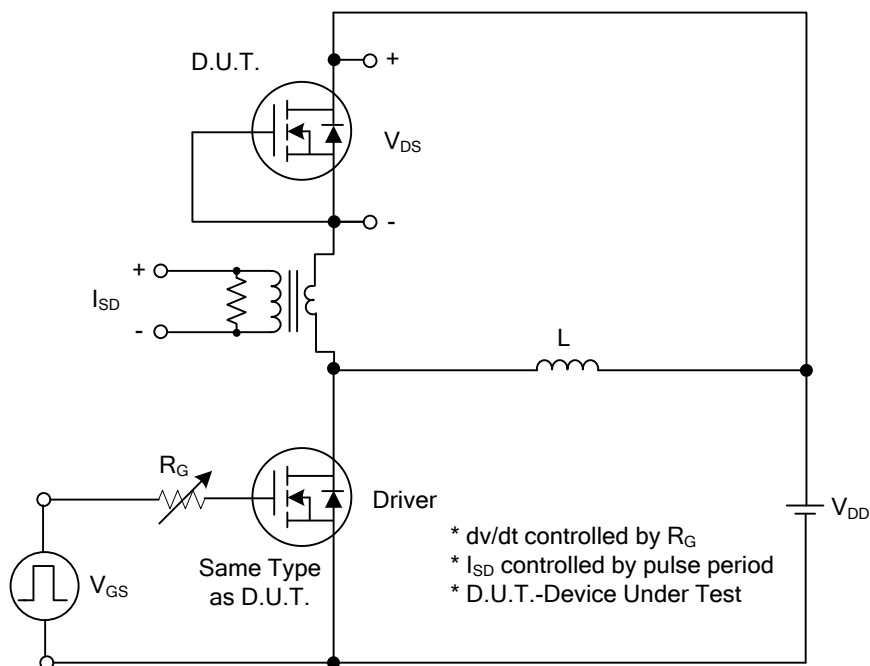
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D = 250μA	600			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =600V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =30V, V _{DS} =0V			100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =2.5A			2.5	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0 MHz		535		pF
Output Capacitance		C _{OSS}			59		pF
Reverse Transfer Capacitance		C _{RSS}			5		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =520V, V _{GS} =10V, I _D =5A I _G =1mA (Note 1, 2)		18		nC
Gate-source Charge		Q _{GS}			7		nC
Gate-Drain Charge		Q _{GD}			4		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =100V, V _{GS} =10V, I _D =5A, R _G =25Ω (Note 1, 2)		8		ns
Rise Time		t _R			16		ns
Turn-off Delay Time		t _{D(OFF)}			32		ns
Fall-Time		t _F			25		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				5	A
Maximum Body-Diode Pulsed Current		I _{SM}				10	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	V _{GS} =0V, I _S =5A			1.4	V
Reverse Recovery Time (Note 1)		t _{rr}	V _{GS} =0V, I _S =5A,		266		ns
Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μs (Note1)		4.9		μC

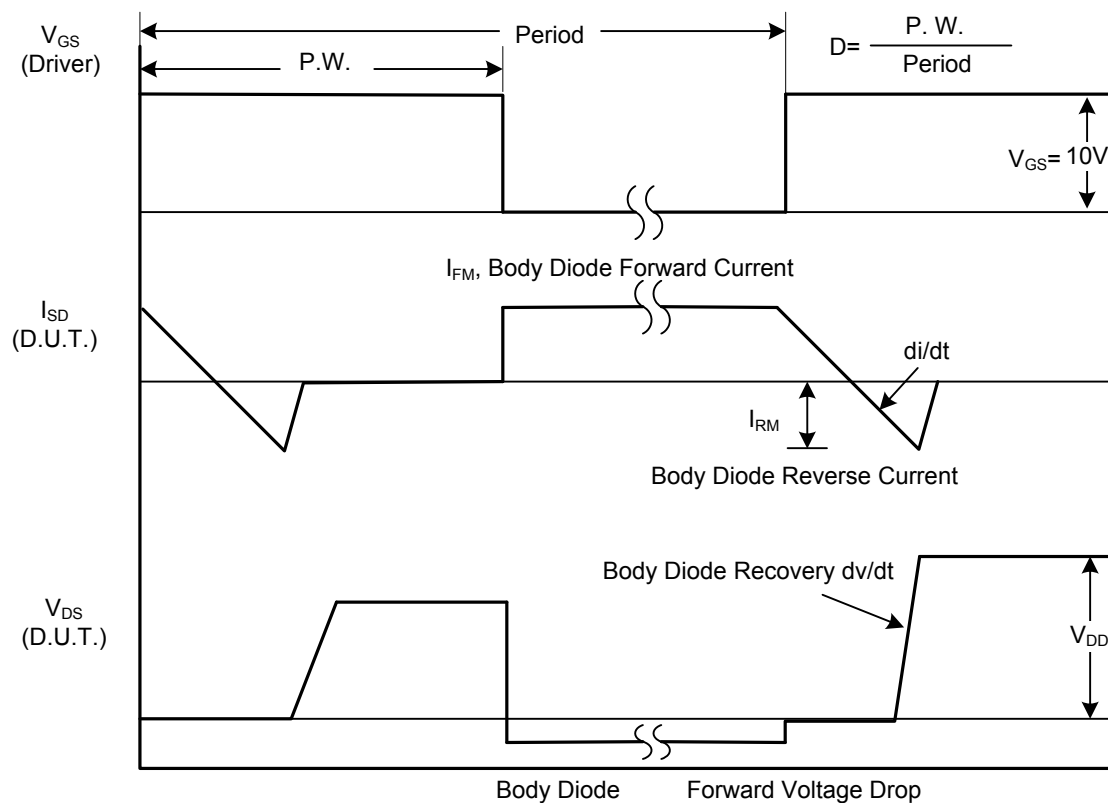
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

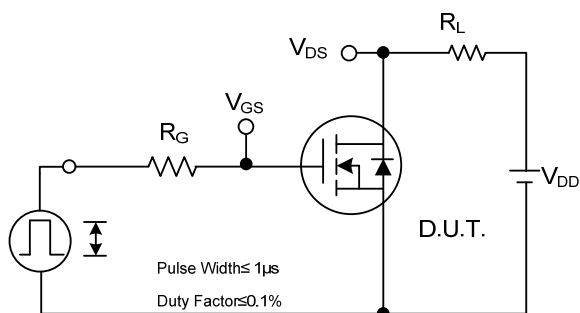


Peak Diode Recovery dv/dt Test Circuit

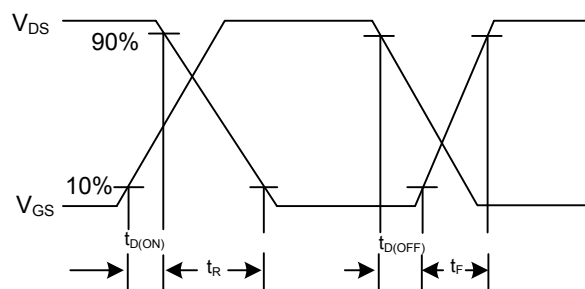


Peak Diode Recovery dv/dt Waveforms

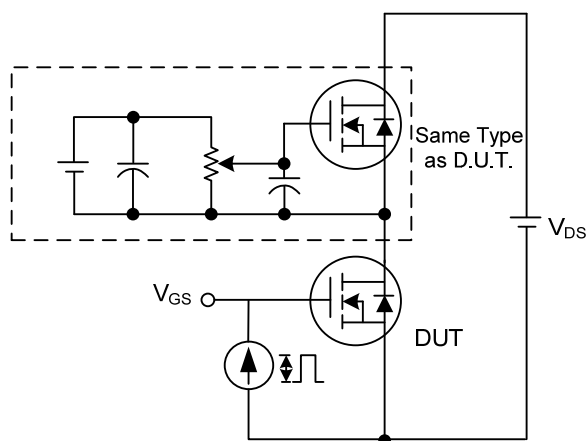
■ TEST CIRCUITS AND WAVEFORMS



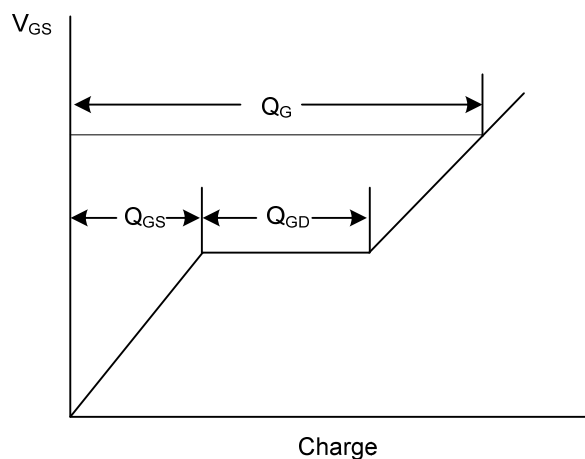
Switching Test Circuit



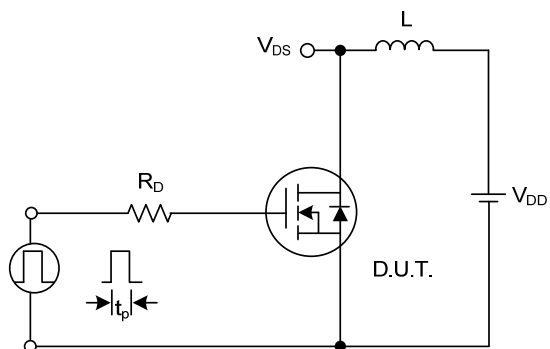
Switching Waveforms



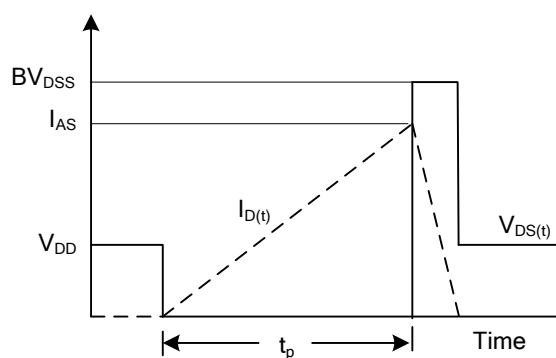
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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