



5NM50A

Preliminary

Power MOSFET

5.0A, 500V N-CHANNEL SUPER-JUNCTION MOSFET

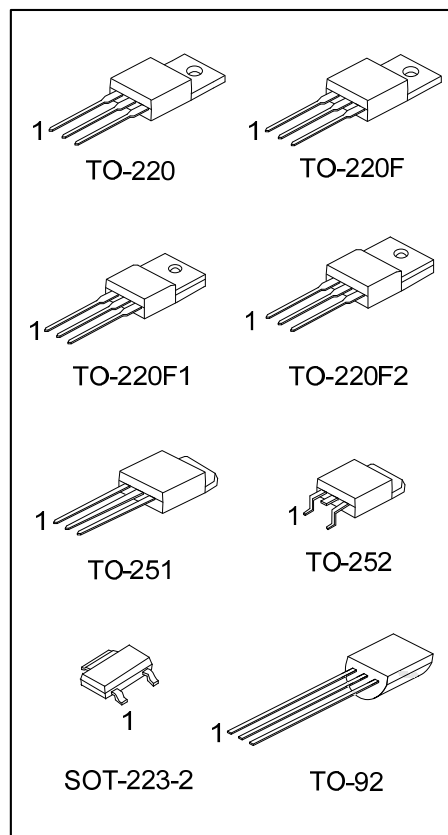
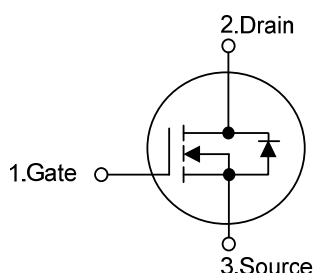
DESCRIPTION

The **UTC 5NM50A** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

FEATURES

- * $R_{DS(ON)} \leq 0.9 \Omega$ @ $V_{GS}=10V$, $I_D=2.5A$
- * Fast Switching Capability
- * Avalanche Energy Specified
- * Improved dv/dt Capability, High Ruggedness

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
5NM50AL-AA2-R	5NM50AG-AA2-R	SOT-223-2	G	D	S	Tape Reel
5NM50AL-TA3-T	5NM50AG-TA3-T	TO-220	G	D	S	Tube
5NM50AL-TF1-T	5NM50AG-TF1-T	TO-220F1	G	D	S	Tube
5NM50AL-TF2-T	5NM50AG-TF2-T	TO-220F2	G	D	S	Tube
5NM50AL-TF3-T	5NM50AG-TF3-T	TO-220F	G	D	S	Tube
5NM50AL-TM3-T	5NM50AG-TM3-T	TO-251	G	D	S	Tube
5NM50AL-TN3-R	5NM50AG-TN3-R	TO-252	G	D	S	Tape Reel
5NM50AL-T92-B	5NM50AG-T92-B	TO-92	G	D	S	Tape Box
5NM50AL-T92-K	5NM50AG-T92-K	TO-92	G	D	S	Bulk

Note: Pin Assignment: G: Gate D: Drain S: Source

5NM50AG-AA2-R		(1) R: Tape Reel, T: Tube, K: Bulk
	(1)Packing Type	(2) AA2: SOT-223-2, TA3: TO-220, TF3: TO-220F,
	(2)Package Type	TF1: TO-220F1, TF2: TO-220F2, TM3: TO-251,
	(3)Green Package	TN3: TO-252, T92: TO-92
		(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING

PACKAGE	MARKING
SOT-223	5NM50A 1 2 3 L: Lead Free G: Halogen Free Date Code
TO-220 / TO-220F TO-220F1 / TO-220F2 TO-251 / TO-252	UTC 5NM50A Lot Code 1 L: Lead Free G: Halogen Free Date Code
TO-92	UTC 5NM50A 1 L: Lead Free G: Halogen Free Date Code

■ **ABSOLUTE MAXIMUM RATINGS** ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 30	V
Drain Current	Continuous	I_D	5	A
	Pulsed (Note 2)	I_{DM}	15	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	144	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.4	V/ns
Power Dissipation	SOT-223-2	P_D	4.2	W
	TO-220		31	W
	TO-220F/TO-220F1 TO-220F2		17	W
	TO-251/TO-252		21	W
	TO-92		3.6	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 144\text{mH}$, $I_{AS} = 1.4\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 5.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient	SOT-223-2	θ_{JA}	150	$^\circ\text{C}/\text{W}$
	TO-220/TO-220F		62.5	$^\circ\text{C}/\text{W}$
	TO-220F1/TO-220F2			
	TO-251/TO-252		110	$^\circ\text{C}/\text{W}$
	TO-92		160	$^\circ\text{C}/\text{W}$
Junction to Case	SOT-223-2	θ_{JC}	29.76 (Note)	$^\circ\text{C}/\text{W}$
	TO-220		4.03	$^\circ\text{C}/\text{W}$
	TO-220F/TO-220F1 TO-220F2		7.35	$^\circ\text{C}/\text{W}$
	TO-251/TO-252		5.95 (Note)	$^\circ\text{C}/\text{W}$
	TO-92		34.72 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	500			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =500V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =30V, V _{DS} =0V			100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.5		4.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =2.5A			0.9	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =50V, f=1MHz		231		pF
Output Capacitance		C _{OSS}			114		pF
Reverse Transfer Capacitance		C _{RSS}			13		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =50V, V _{GS} =10V, I _D =2.5A (Note 1, 2)		17		nC
Gate to Source Charge		Q _{GS}			5		nC
Gate to Drain Charge		Q _{GD}			7		nC
Turn-ON Delay Time (Note 1)		t _{D(ON)}	V _{DS} =100V, V _{GS} =10V, I _D =5.0A, R _G =25Ω (Note 1, 2)		9		ns
Rise Time		t _R			22		ns
Turn-OFF Delay Time		t _{D(OFF)}			32		ns
Fall-Time		t _F			23		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				5	A
Maximum Body-Diode Pulsed Current		I _{SM}				15	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =5.0A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)		t _{rr}	I _S =5.0A, V _{GS} =0V,		196		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μs		1.5		μC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

D.U.T.

V_{DS}

I_{SD}

L

V_{DD}

R_G

Driver

Same Type as D.U.T.

V_{GS}

- * dv/dt controlled by R_G
- * I_{SD} controlled by pulse period
- * D.U.T.-Device Under Test

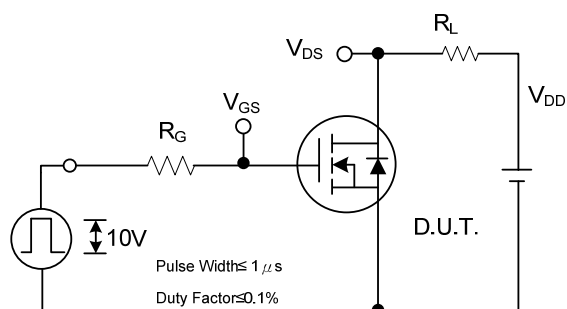
Timing diagram for a MOSFET switching a load inductor. The diagram shows three waveforms: V_{GS} (Driver), I_{SD} (D.U.T.), and V_{DS} (D.U.T.).

- V_{GS} (Driver): A square wave with pulse width (P.W.) and period (Period). The duty cycle is defined as $D = \frac{P.W.}{Period}$. The gate-source voltage is $V_{GS} = 10V$.
- I_{SD} (D.U.T.): The drain current. It shows forward current I_{FM} (Body Diode Forward Current) during the on-time and reverse current I_{RM} (Body Diode Reverse Current) during the off-time. The reverse current slope is labeled di/dt .
- V_{DS} (D.U.T.): The drain-source voltage. It shows the voltage across the MOSFET, including the body diode recovery dv/dt during the off-time. The drain-source voltage is V_{DD} .

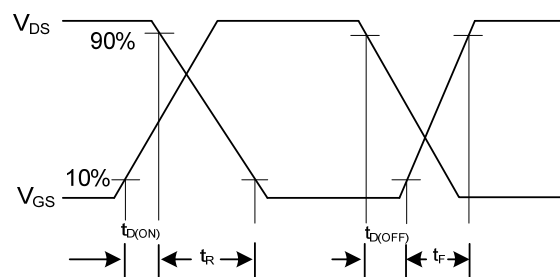
Labels at the bottom indicate the regions: Body Diode Forward Voltage Drop and Body Diode Recovery dv/dt .

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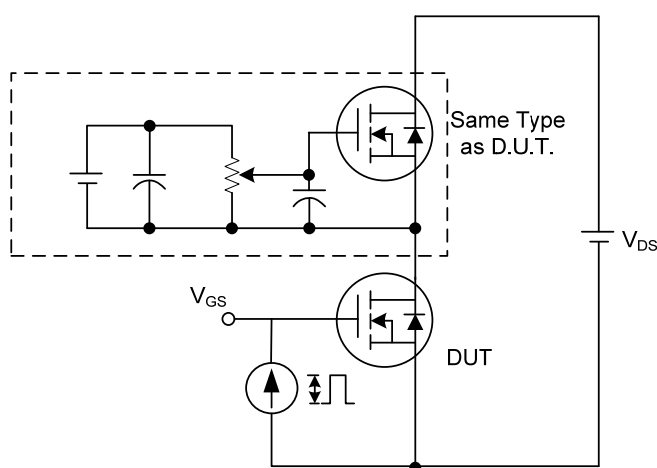
■ TEST CIRCUITS AND WAVEFORMS



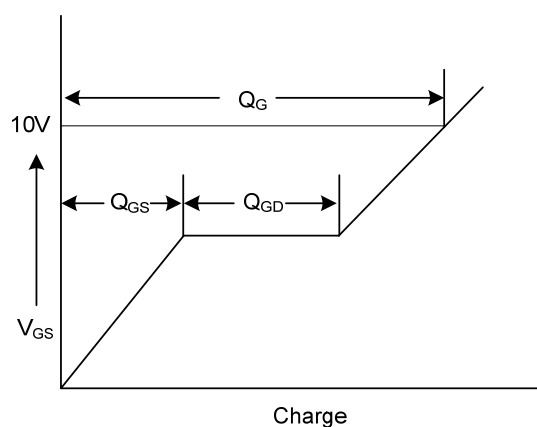
Switching Test Circuit



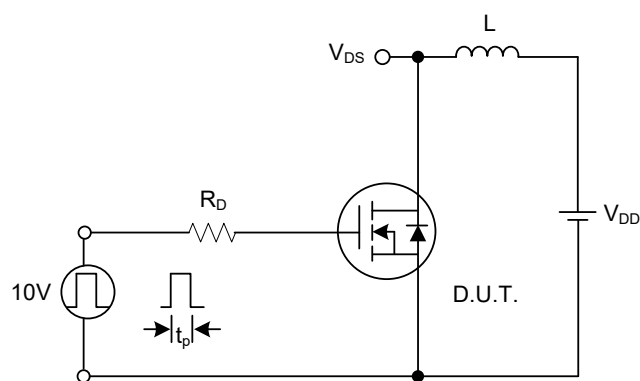
Switching Waveforms



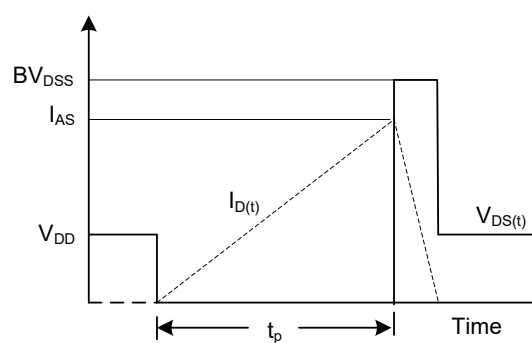
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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