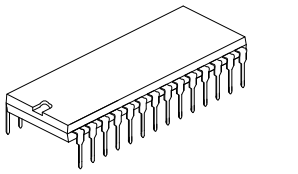
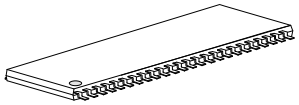
RAM MAPPLING 32×4 LCD CONTROLLER FOR I/O µC



DIP-28



SSOP-48

■ DESCRIPTION

The UTC **6621** is a 128 patterns (32×4), memory mapping, and multi-function LCD driver. Profit from its S/W configuration feature, the UTC **6621** is suitable for multiple LCD applications including LCD modules and display sub-systems, and only three or four lines are required for the interface between the UTC **6621** and its host controller. A power down command is introduced in the UTC **6621** to reduce power consumption.

■ FEATURES

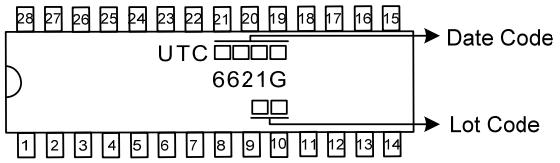
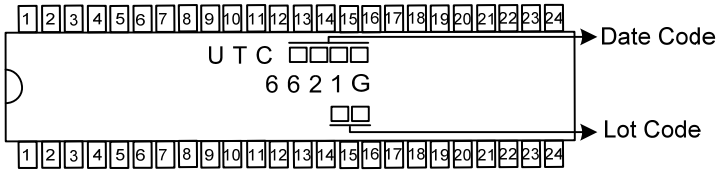
* Operating voltage range: 2.4V~5.2V
* External 32.768kHz crystal or 256kHz frequency source input
* Built-in 256kHz RC oscillator
* Internal time base frequency sources
* Two selectable bias (1/2 or 1/3), and three selectable duty LCD applications (1/2 or 1/3 or 1/4).
* Two selectable buzzer frequencies (2kHz/4kHz)
* Power down command reduces power consumption
* Built-in time base generator and WDT
* Time base or WDT overflow output
* 32×4 LCD driver
* 8 kinds of time base/WDT clock sources
* Built-in 32×4 bit display RAM
* 3-wire serial interface
* Software configuration feature
* Internal LCD driving frequency source
* Data mode and command mode instructions
* VLCD pin for adjusting LCD operating voltage
* R/W address auto increment
* Three data accessing modes

■ ORDERING INFORMATION

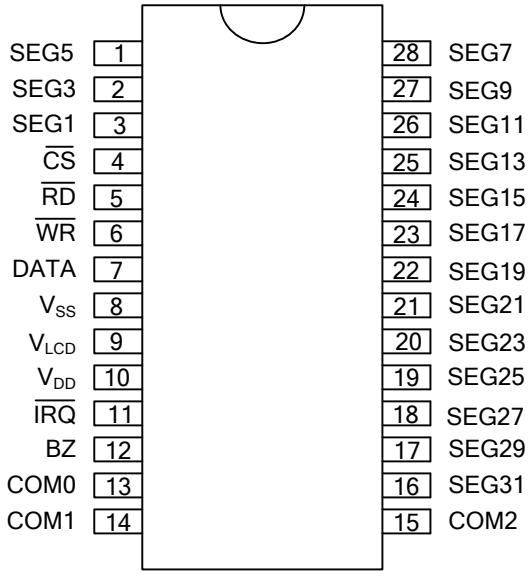
Ordering Number	Package	Packing
6621G-D28-T	DIP-28	Tube
6621G-R48-T	SSOP-48	Tape Reel

6621G-D28-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube, R: Tape Reel (2) D28: DIP-28, R48: SSOP-48 (3) G: Halogen Free and Lead Free

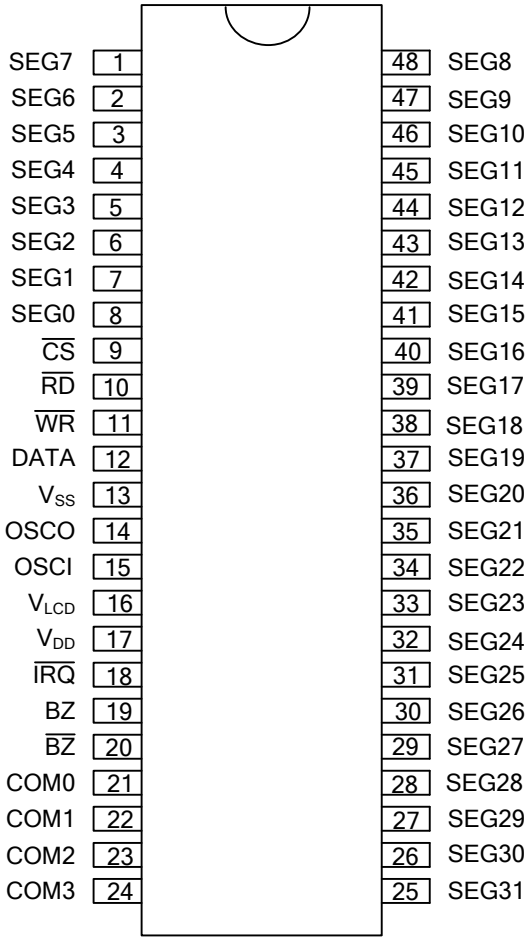
■ MARKING

PACKAGE	MARKING
DIP-28	
SSOP-48	

■ PIN CONFIGURATION



DIP-28

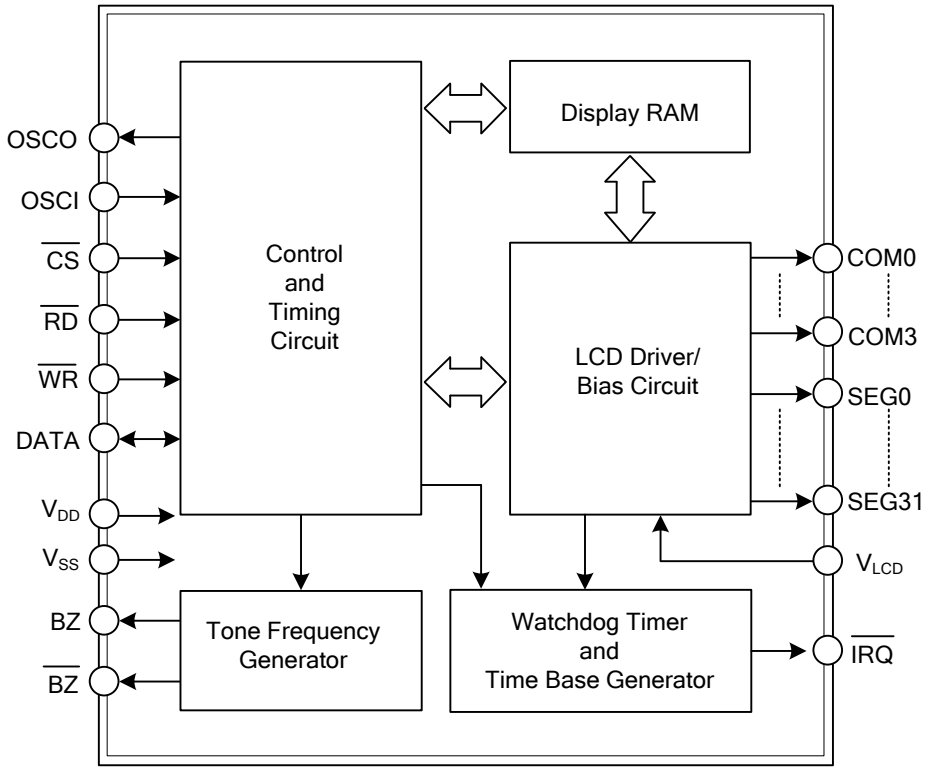


SSOP-48

■ PIN DESCRIPTION

PIN NO.		I/O	PIN NAME	DESCRIPTION
DIP-28	SSOP-48			
1~3, 16~28	1~8, 25~48	O	SEG0~SEG31	LCD segment outputs
4	9	I	$\overline{CS}$	Chip selection input with pull-high resistor
5	10	I	$\overline{RD}$	READ clock input with pull-high resistor
6	11	I	$\overline{WR}$	WRITE clock input with pull-high resistor
7	12	I/O	DATA	Serial data input/output with pull-high resistor
8	13		V_{SS}	Negative power supply, ground
9	16	I	V_{LCD}	LCD power input
10	17		V_{DD}	Positive power supply
11	18	O	$\overline{IRQ}$	Time base or WDT overflow flag, NMOS open drain output
12	19	O	BZ	2kHz or 4kHz tone frequency output pair
-	20	O	$\overline{BZ}$	
13~15	21~24	O	COM0~COM3	LCD common outputs
-	14	O	OSCO	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
-	15	I	OSCI	

■ BLOCK DIAGRAM



Note: $\overline{CS}$: Chip selection

BZ, $\overline{BZ}$: Tone outputs

$\overline{WR}$, $\overline{RD}$, DATA: Serial interface

COM0~COM3, SEG0~SEG31: LCD outputs

$\overline{IRQ}$: Time base or WDT overflow output

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3~5.5	V
Input Voltage		V_{SS}-0.3~V_{DD}+0.3	V
Operating Temperature	T_{OPR}	-25~+75	°C
Storage Temperature	T_{STG}	-50~+125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

D.C. Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}			2.4		5.2	V
Operating Current	I_{DD1}	V_{DD}=3V	No Load/LCD ON On-Chip RC Oscillator		150	300	μA
		V_{DD}=5V			300	600	μA
Operating Current	I_{DD2}	V_{DD}=3V	No Load/LCD ON Crystal Oscillator		60	120	μA
		V_{DD}=5V			120	240	μA
Operating Current	I_{DD3}	V_{DD}=3V	No Load/LCD ON External Clock Source		100	200	μA
		V_{DD}=5V			200	400	μA
Standby Current	I_{STB}	V_{DD}=3V	No Load Power Down Mode		0.1	5	μA
		V_{DD}=5V			0.3	10	μA
Input Low Voltage	V_{IL}	V_{DD}=3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0		0.6	V
		V_{DD}=5V		0		1.0	V
Input High Voltage	V_{IH}	V_{DD}=3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4		3.0	V
		V_{DD}=5V		4.0		5.0	V
DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	I_{OL1}	V_{DD}=3V, V_{OL}=0.3V		0.5	1.2		mA
		V_{DD}=5V, V_{OL}=0.5V		1.3	2.6		mA
DATA, BZ, $\overline{BZ}$	I_{OH1}	V_{DD}=3V, V_{OH}=2.7V		-0.4	-0.8		mA
		V_{DD}=5V, V_{OH}=4.5V		-0.9	-1.8		mA
LCD Common Sink Current	I_{OL2}	V_{DD}=3V, V_{OL}=0.3V		80	150		μA
		V_{DD}=5V, V_{OL}=0.5V		150	250		μA
LCD Common Source Current	I_{OH2}	V_{DD}=3V, V_{OH}=2.7V		-80	-120		μA
		V_{DD}=5V, V_{OH}=4.5V		-120	-200		μA
LCD Segment Sink Current	I_{OL3}	V_{DD}=3V, V_{OL}=0.3V		60	120		μA
		V_{DD}=5V, V_{OL}=0.5V		120	200		μA
LCD Segment Source Current	I_{OH3}	V_{DD}=3V, V_{OH}=2.7V		-40	-70		μA
		V_{DD}=5V, V_{OH}=4.5V		-70	-100		μA
Pull-High Resistor	R_{PH}	V_{DD}=3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	40	80	150	KΩ
		V_{DD}=5V		30	60	100	KΩ

■ ELECTRICAL CHARACTERISTICS

A.C. Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock	f_{SYS1}	V_{DD}=3V	On-Chip RC Oscillator		256		kHz
		V_{DD}=5V			256		kHz
System Clock	f_{SYS2}	V_{DD}=3V	Crystal Oscillator		32.768		kHz
		V_{DD}=5V			32.768		kHz
System Clock	f_{SYS3}	V_{DD}=3V	External Clock Source		256		kHz
		V_{DD}=5V			256		kHz
LCD Clock	f_{LCD}	On-Chip RC Oscillator			f_{SYS1}/1024		Hz
		Crystal Oscillator			f_{SYS2}/128		Hz
		External Clock Source			f_{SYS3}/1024		Hz
LCD Common Period	t_{COM}	n: Number of COM			n/f_{LCD}		s
Serial Data Clock ($\overline{WR}$ Pin)	f_{CLK1}	V_{DD}=3V	Duty Cycle 50%			150	kHz
		V_{DD}=5V				300	kHz
Serial Data Clock ($\overline{RD}$ Pin)	f_{CLK2}	V_{DD}=3V	Duty Cycle 50%			75	kHz
		V_{DD}=5V				150	kHz
Tone Frequency	f_{TONE}	On-Chip RC Oscillator			2.0 or 4.0		kHz
Serial Interface Reset Pulse Width (Figure 3)	t_{CS}	$\overline{CS}$			250		ns
$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	t_{CLK}	V_{DD}=3V	Write Mode	3.34			μs
			Read Mode	6.67			μs
		V_{DD}=5V	Write Mode	1.67			μs
			Read Mode	3.34			μs
Rise/Fall Time Serial Data Clock Width (Figure 1)	t_r,t_f	V_{DD}=3V			120		ns
		V_{DD}=5V					
Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	t_{su}	V_{DD}=3V			120		ns
		V_{DD}=5V					
Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	t_h	V_{DD}=3V			120		ns
		V_{DD}=5V					
Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	t_{su1}	V_{DD}=3V			100		ns
		V_{DD}=5V					
Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	t_{h1}	V_{DD}=3V			100		ns
		V_{DD}=5V					

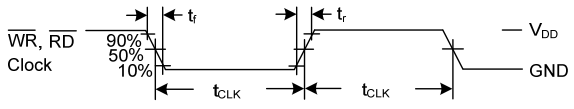


Figure 1

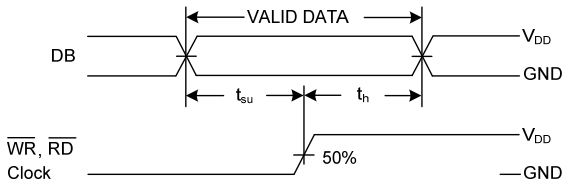


Figure 2

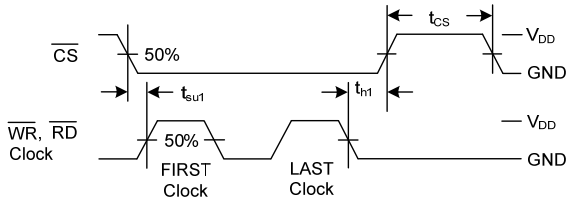
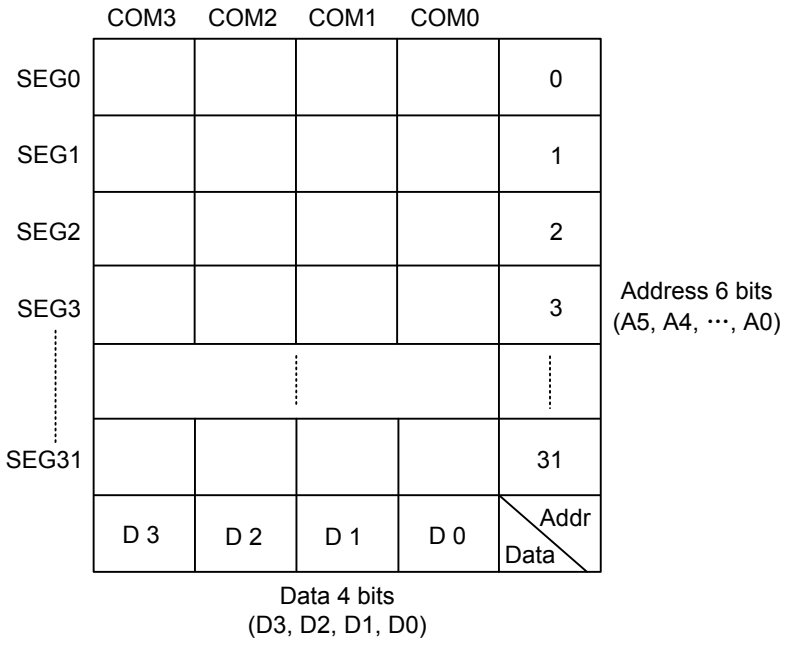


Figure 3

■ FUNCTIONAL DESCRIPTION

Display memory - RAM

The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:



RAM mapping

System oscillator

The UTC **6621** system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the UTC **6621** is at the SYS DIS state.

Time base and Watchdog Timer (WDT)

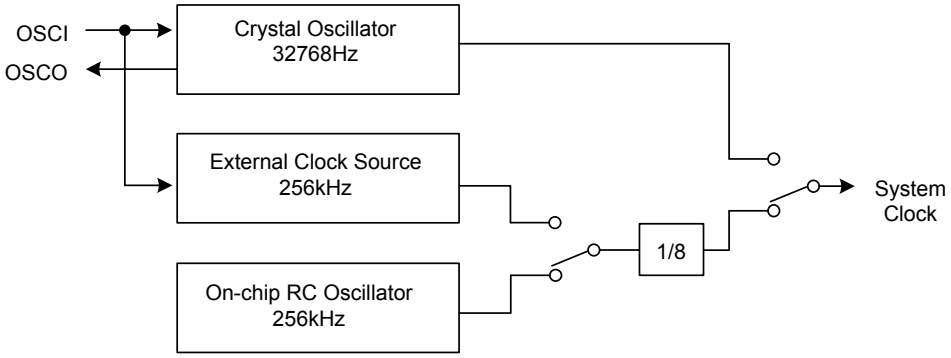
The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other sub-systems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the $\overline{IRQ}$ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

$$f_{WDT} = \frac{32kHz}{2^n}$$

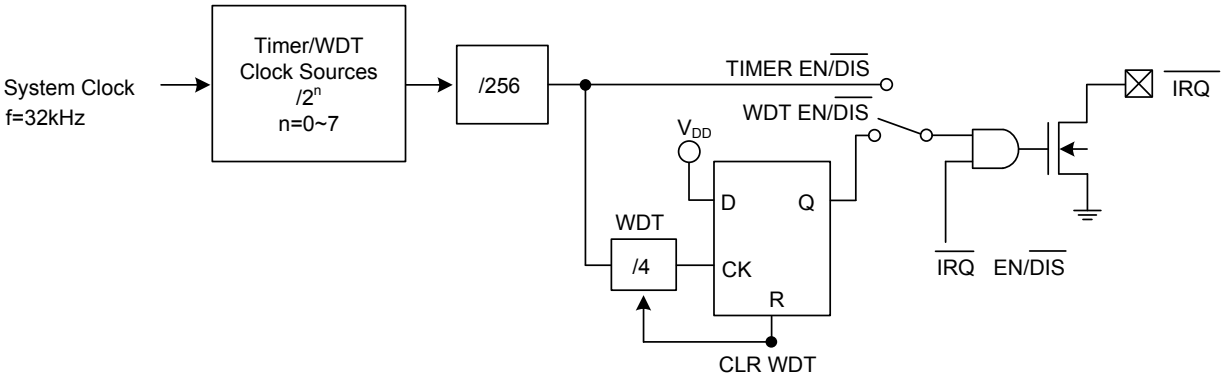
■ FUNCTIONAL DESCRIPTION(Cont.)

where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256kHz.

If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the $\overline{IRQ}$ pin). After the TIMER EN command is transferred, the WDT is disconnected from the $\overline{IRQ}$ pin, and the output of the time base generator is connected to the $\overline{IRQ}$ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is cleared by executing the CLR WDT or the CLR.



System oscillator configuration



Timer and WDT configurations

Name	Command Code	Function
LCD OFF	10000000010X	Turn off LCD outputs
LCD ON	10000000011X	Turn on LCD outputs
BIAS & COM	1000010abXcX	C=0:1/2 bias option C=1:1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option

■ FUNCTIONAL DESCRIPTION(Cont.)

TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the $\overline{IRQ}$ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued. After the $\overline{IRQ}$ output is disabled the $\overline{IRQ}$ pin will remain at the floating state. The $\overline{IRQ}$ output can be enabled or disabled by executing the $\overline{IRQ}$ EN or the $\overline{IRQ}$ DIS command, respectively. The $\overline{IRQ}$ EN makes the output of the time base generator or of the WDT time-out flag appear on the $\overline{IRQ}$ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the UTC **6621** will continue working until system power fails or the external clock source is removed. After the system power on, the $\overline{IRQ}$ will be disabled.

Tone output

A simple tone generator is implemented in the UTC **6621**. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will re-main at low level.

LCD driver

The UTC **6621** is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the UTC **6621** suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 1 0 0, namely 1 0 0, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands, the UTC **6621** can be compatible with most types of LCD panels.

Command format

The UTC **6621** can be configured by the S/W setting. There are two mode commands to configure the UTC **6621** resources and to transfer the LCD display data. The configuration mode of the UTC **6621** is called command mode, and its command mode ID is 1 0 0. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

■ FUNCTIONAL DESCRIPTION(Cont.)

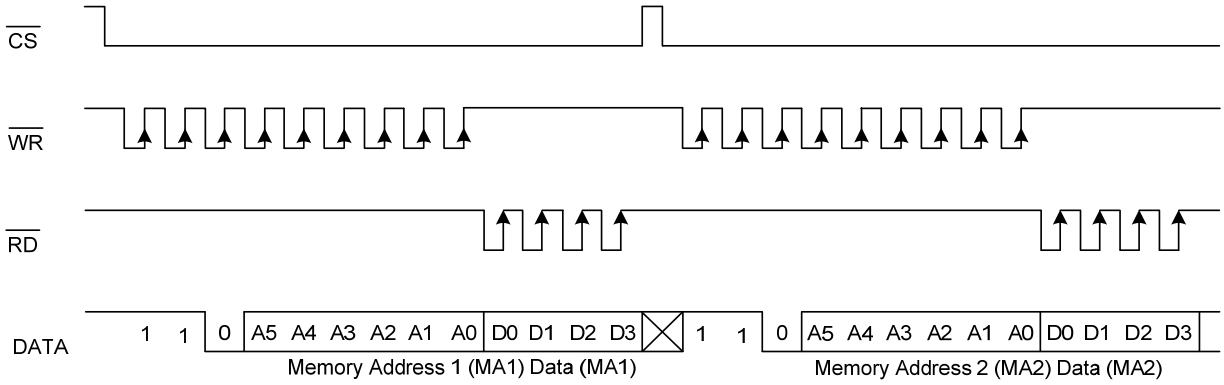
The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely 1 0 0, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. Once the $\overline{CS}$ pin returns to "0" a new operation mode ID should be issued first.

Interfacing

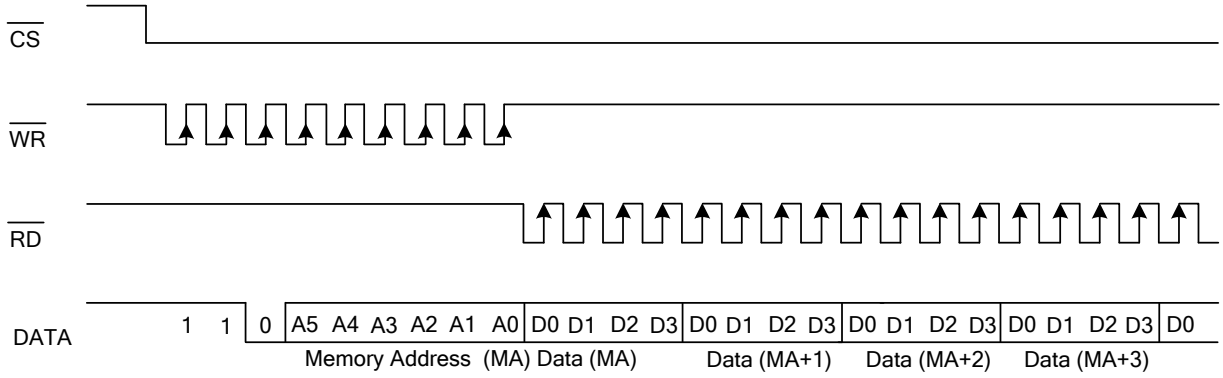
Only four lines are required to interface with the UTC **6621**. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the UTC **6621**. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the UTC **6621** are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the UTC **6621**. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the UTC **6621** on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the UTC **6621**. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the $\overline{IRQ}$ pin of the UTC **6621**.

■ TIMING DIAGRAMS

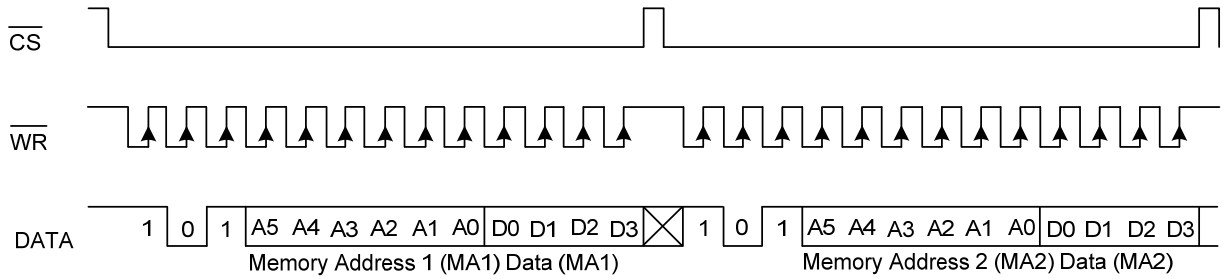
READ mode (command code: 110)



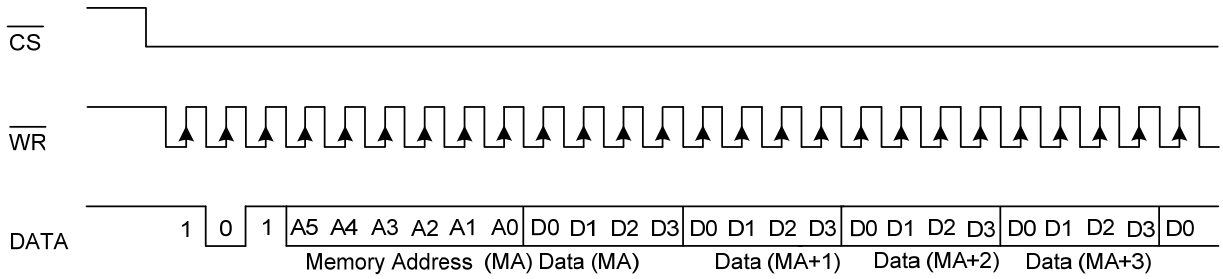
READ mode (successive address reading)



WRITE mode (command code: 101)

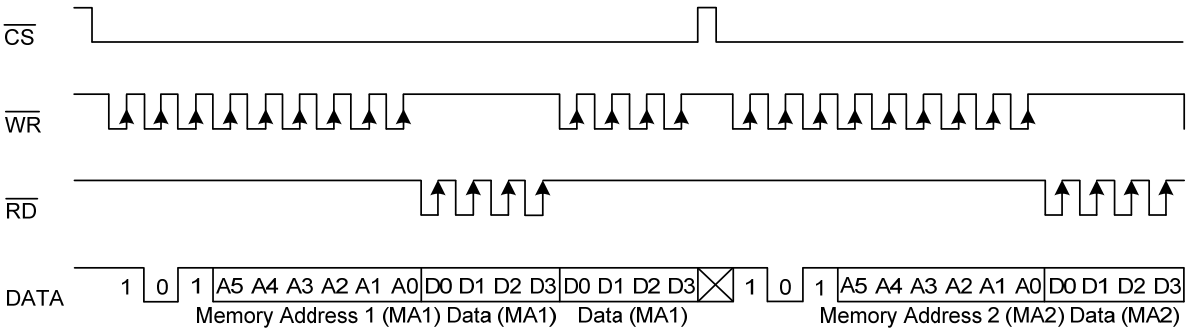


WRITE mode (successive address writing)

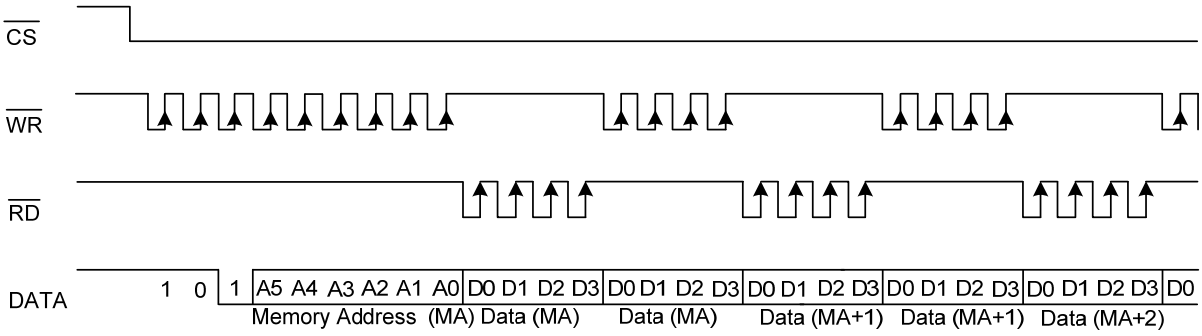


■ TIMING DIAGRAMS(Cont.)

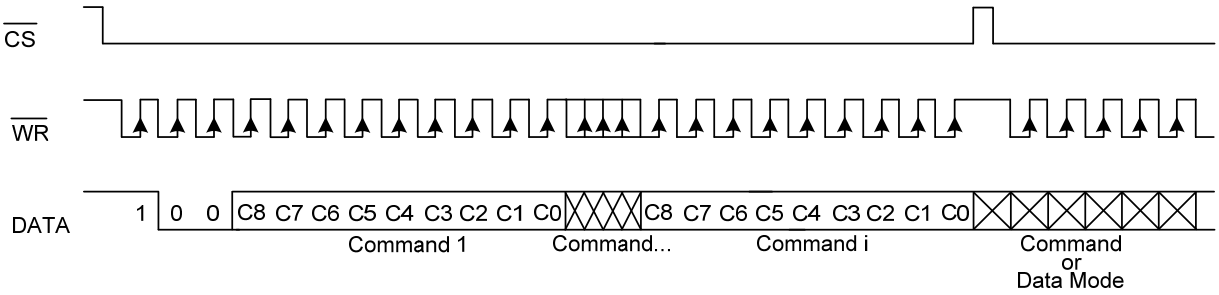
READ-MODIFY-WRITE mode (command code: 101)



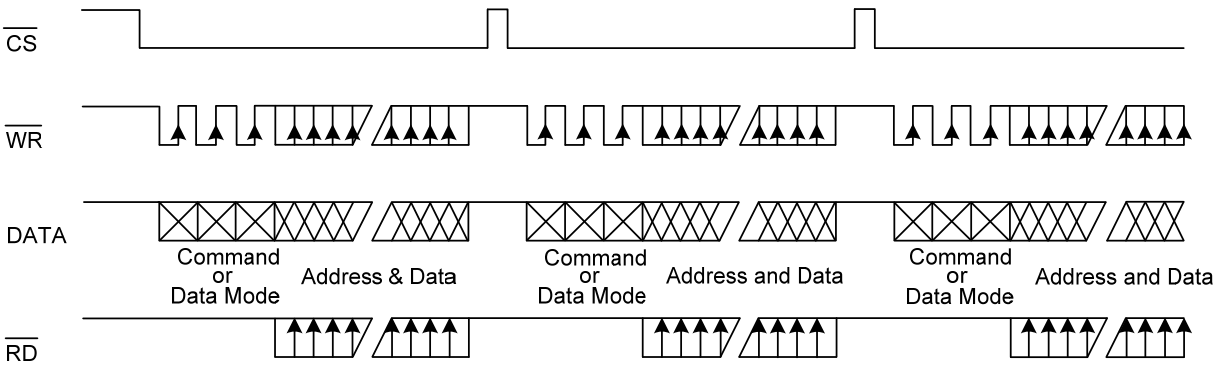
READ-MODIFY-WRITE mode (successive address accessing)



Command mode (command code:100)



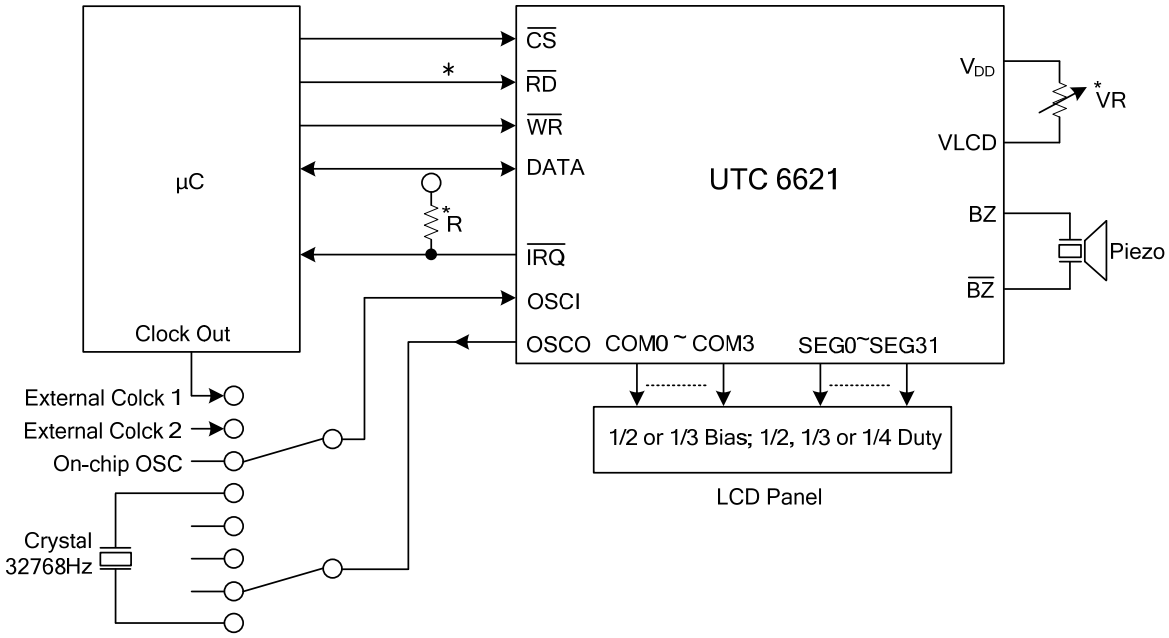
Mode (data and command mode)



Note: It is recommended that the host controller should read in the data from the DATA line between the rising edge of the $\overline{RD}$ line and the falling edge of the next $\overline{RD}$ line.

■ TYPICAL APPLICATION CIRCUIT

Host controller with an UTC **6621** display system



Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the µC.
The voltage applied to VLCD pin must be lower than V_{DD}.
Adjust V_R to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR=15kw ± 20%.
Adjust R (external pull-high resistance) to fit user's time base clock.