



7NM100

Power MOSFET

7.0A, 1000V N-CHANNEL SUPER-JUNCTION MOSFET

DESCRIPTION

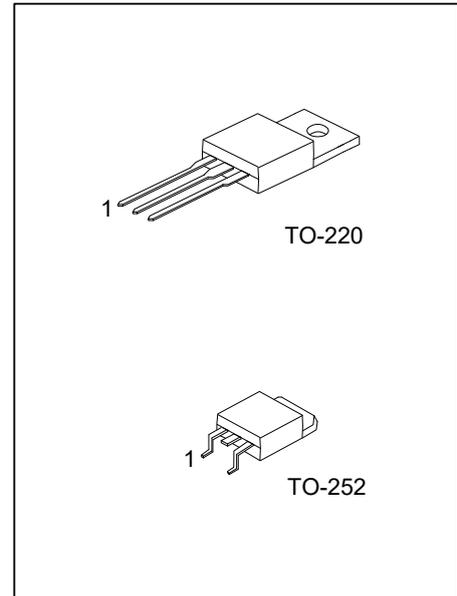
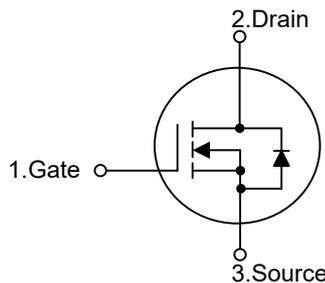
The UTC **7NM100** is an Super Junction MOSFET Structure. It uses UTC advanced planar stripe, DMOS technology to provide customers perfect switching performance, minimal on-state resistance.

The UTC **7NM100** is universally applied in electronic lamp ballasts based on half bridge topology, high efficiency switched mode power supplies, active power factor correction, etc.

FEATURES

- * $R_{DS(ON)} \leq 1.35 \Omega @ V_{GS}=10V, I_D=3.5A$
- * High switching speed
- * High breakdown voltage

SYMBOL



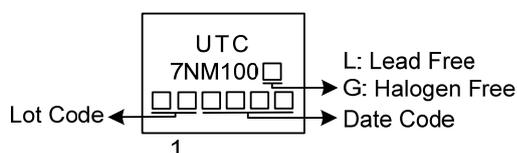
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7NM100L-TA3-T	7NM100G-TA3-T	TO-220	G	D	S	Tube
7NM100L-TN3-R	7NM100G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>7NM100G-TA3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TA3: TO-220, TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	1000	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	7	A
	Pulsed	I_{DM}	21	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	200	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.6	V/ns
Power Dissipation	TO-220	P_D	95	W
	TO-252		38	W
Junction Temperature		T_J	-55 ~ +150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Repetitive Rating: Pulse width limited by maximum junction temperature
 3. $L = 100\text{mH}$, $I_{AS} = 2\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$ Starting $T_J = 25^\circ\text{C}$
 4. $I_{SD} \leq 7.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
	TO-252		110	$^\circ\text{C}/\text{W}$
Junction to Case	TO-220	θ_{JC}	1.316	$^\circ\text{C}/\text{W}$
	TO-252		3.2 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

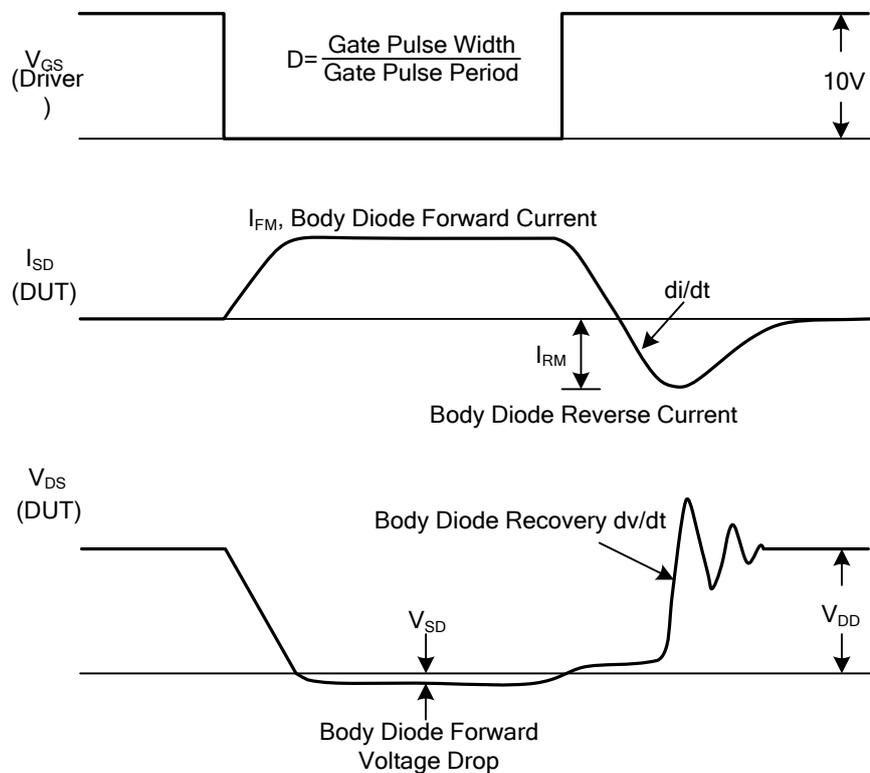
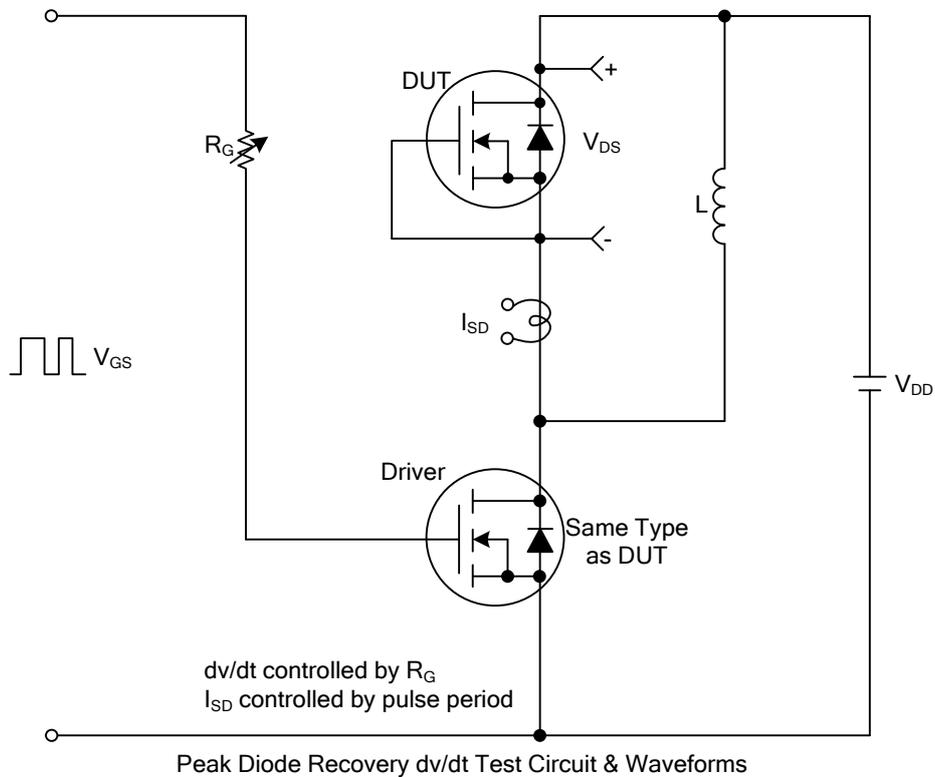
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =0.25mA, V _{GS} =0V	1000			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =1000V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}			+100	nA
	Reverse				V _{GS} =+30V, V _{DS} =0V	-100
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.5		4.5	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =3.5A			1.35	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =50V, f=1.0MHz		650		pF
Output Capacitance	C _{OSS}			47		pF
Reverse Transfer Capacitance	C _{RSS}			3		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =800V, V _{GS} =10V, I _D =7.0A, (Note 1,2)		40		nC
Gate to Source Charge	Q _{GS}			10		nC
Gate to Drain Charge	Q _{GD}			15		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =7.0A, R _G =25Ω (Note 1,2)		7		ns
Rise Time	t _R			16.5		ns
Turn-OFF Delay Time	t _{D(OFF)}			28		ns
Fall-Time	t _F			20		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				7	A
Maximum Body-Diode Pulsed Current	I _{SM}				21	A
Drain-Source Diode Forward Voltage	V _{SD}	I _F =7.0A, V _{GS} =0V			1.4	V
Reverse Recovery Time	t _{rr}	I _S =7.0A, V _{GS} =0V,		516		ns
Reverse Recovery Charge	Q _{rr}	dI _F /dt=100A/μs (Note 1)		6.6		μC

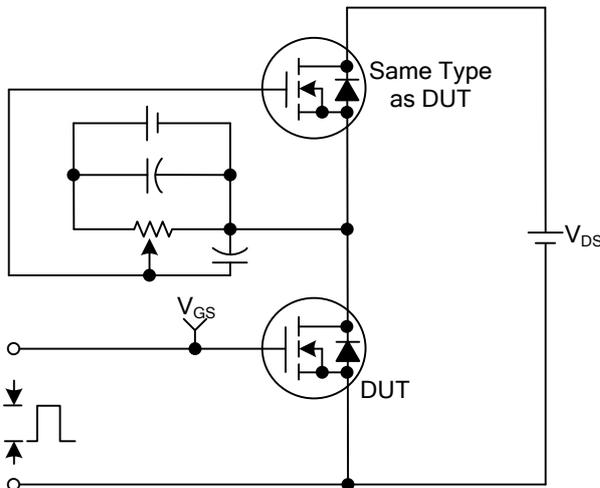
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

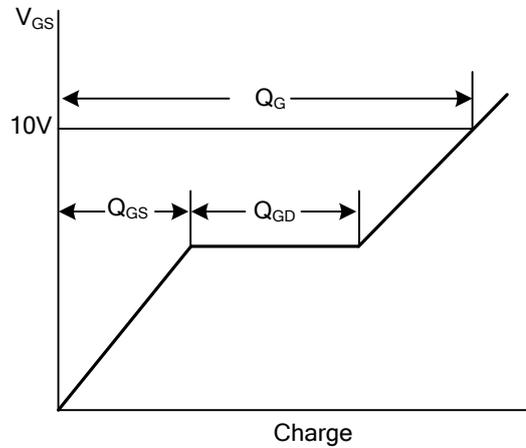
■ TEST CIRCUITS AND WAVEFORMS



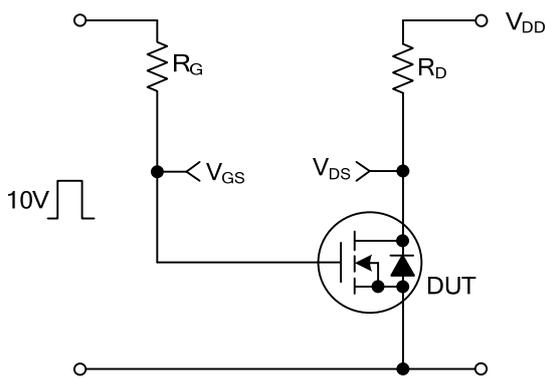
TEST CIRCUITS AND WAVEFORMS



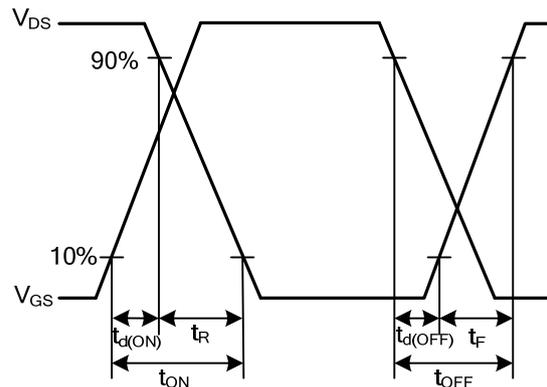
Gate Charge Test Circuit



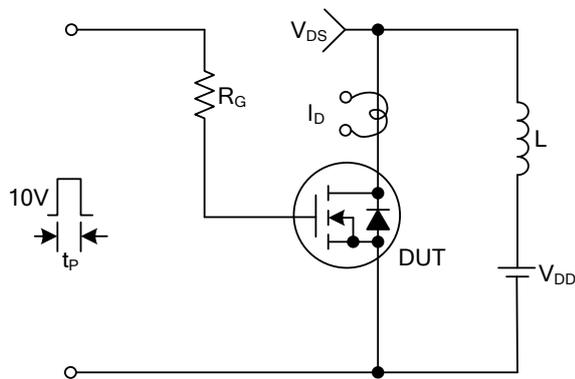
Gate Charge Waveforms



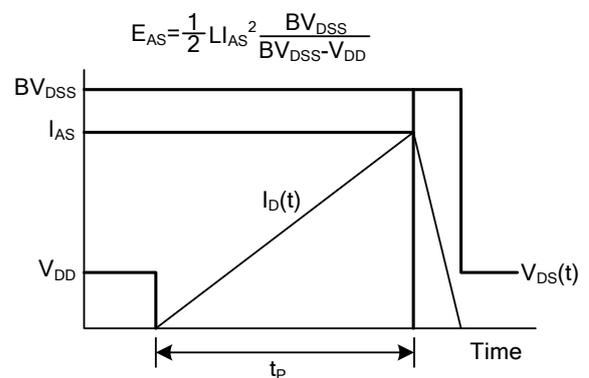
Resistive Switching Test Circuit



Resistive Switching Waveforms

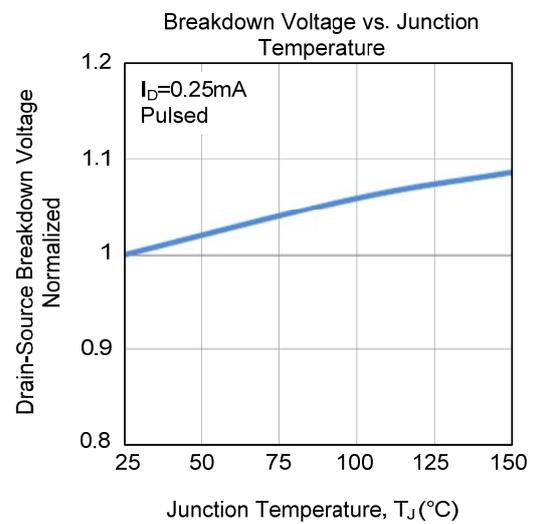
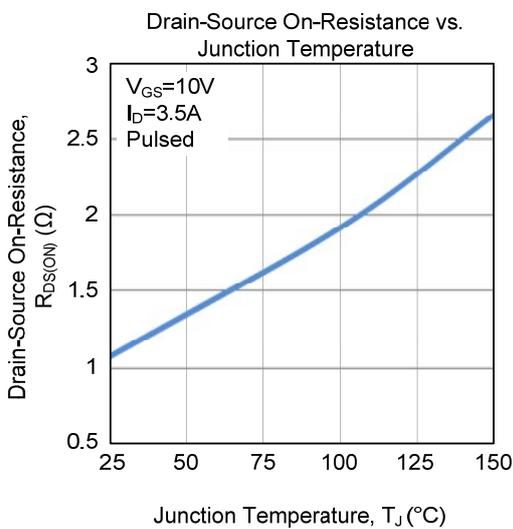
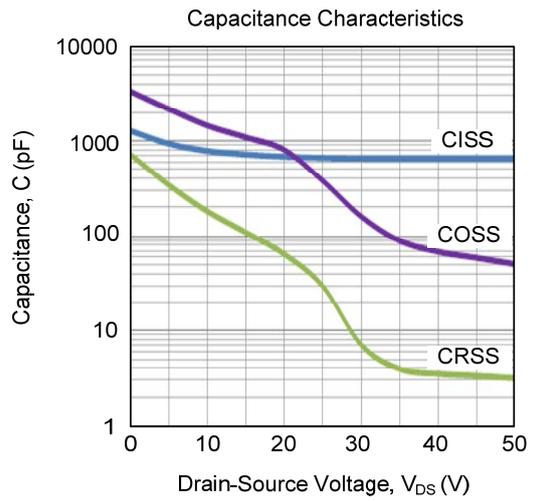
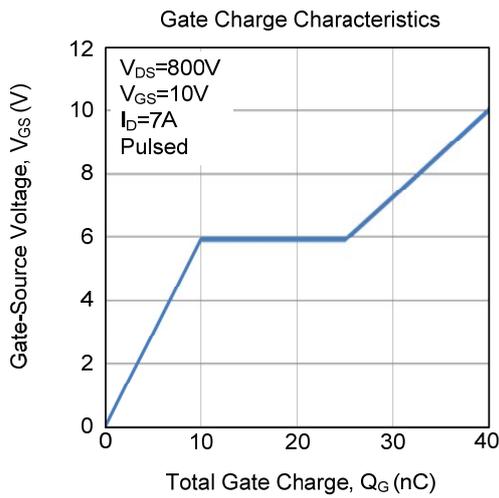
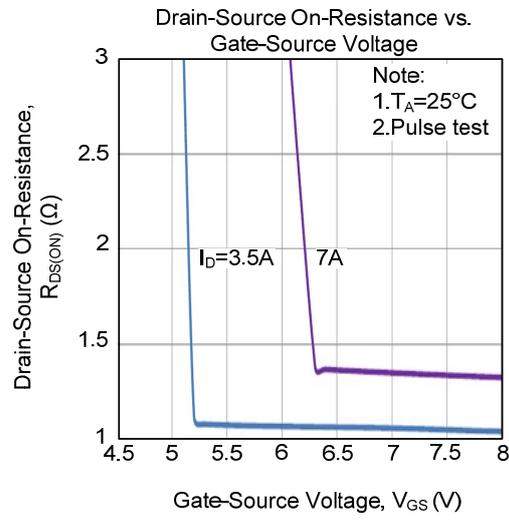
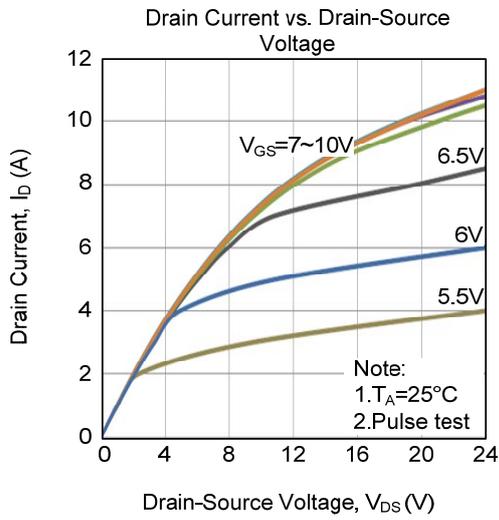


Unclamped Inductive Switching Test Circuit

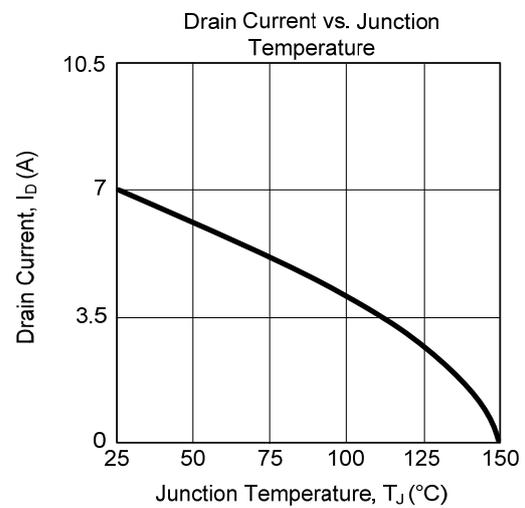
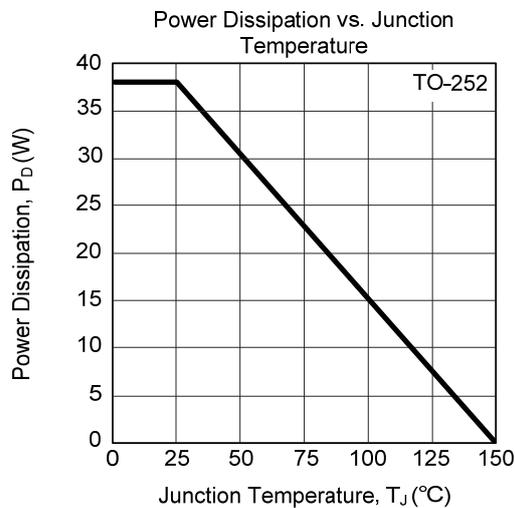
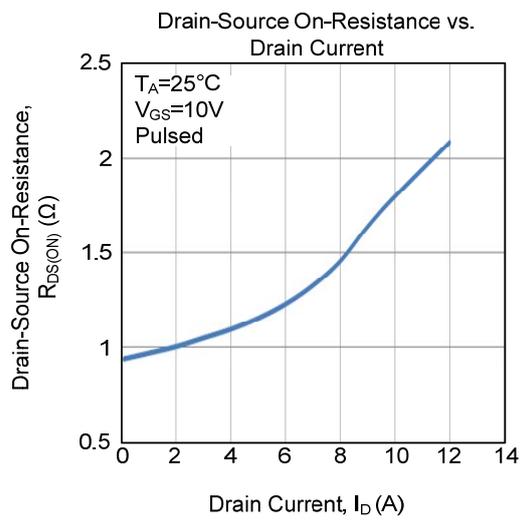
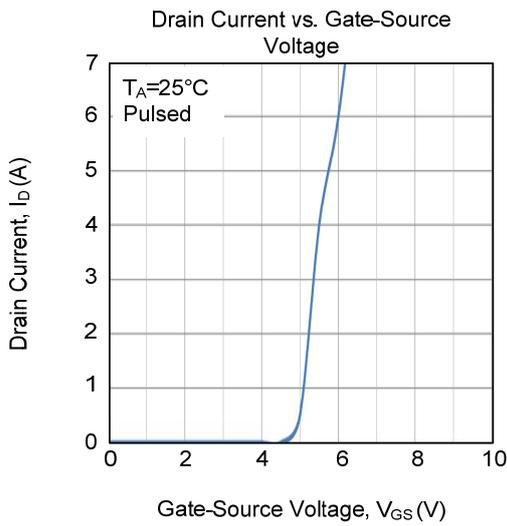
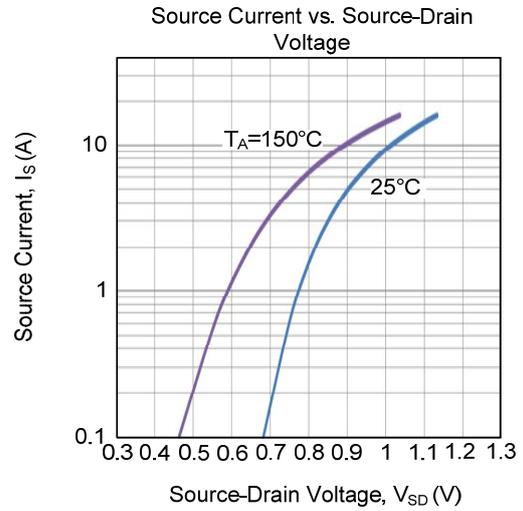
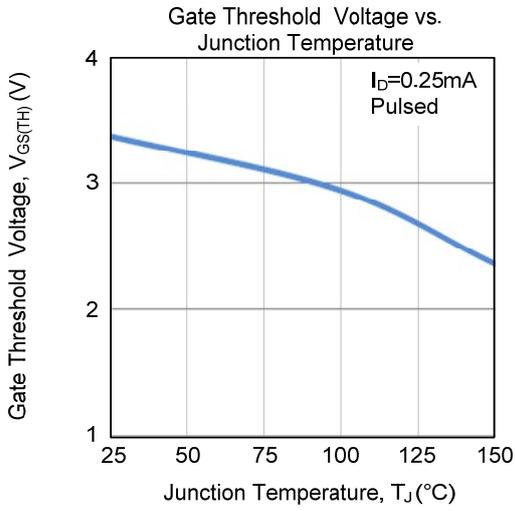


Unclamped Inductive Switching Waveforms

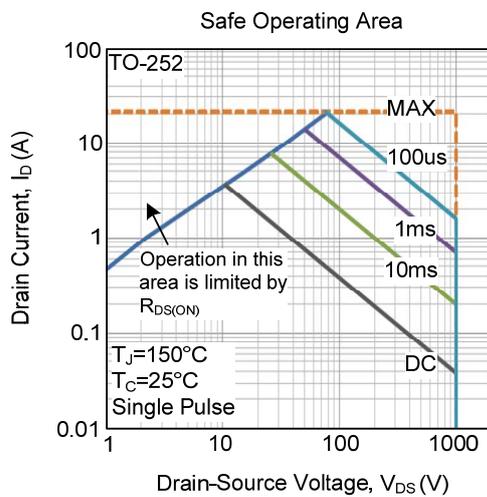
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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