



7P50

POWER MOSFET

-7.0A, -500V P-CHANNEL POWER MOSFET

DESCRIPTION

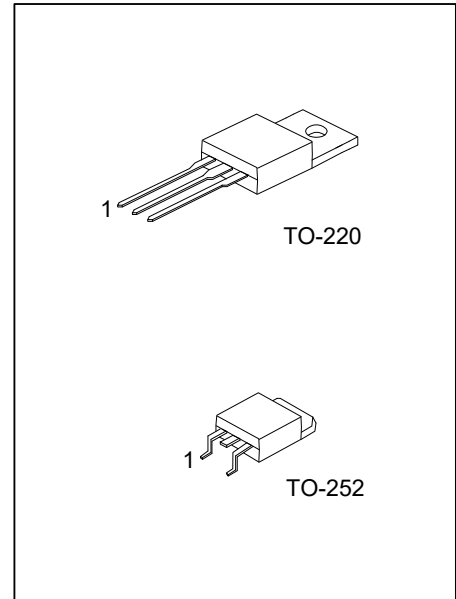
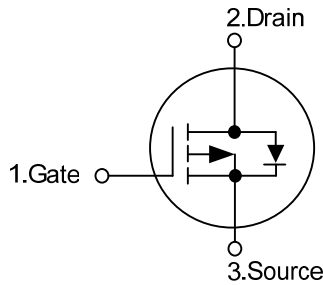
The UTC **7P50** is a P-channel MOS Field Effect Transistor. it uses UTC's advanced technology to provide the customers with high switching speed and a minimum on-state resistance.

The UTC **7P50** is suitable for high voltage switching applications.

FEATURES

- * $R_{DS(ON)} \leq 1.8 \Omega$ @ $V_{GS} = -10V$, $I_D = -3.5A$
- * High switching speed
- * Low input capacitance

SYMBOL



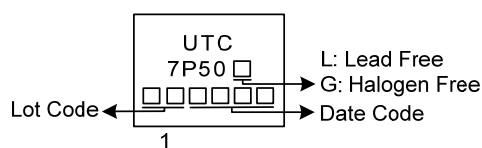
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7P50L-TA3-T	7P50G-TA3-T	TO-220	G	D	S	Tube
7P50L-TN3-R	7P50G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

7P50G-TA3-T (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TN3: TO-252 (3) G: Halogen Free and Lead Free L: Lead Free
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MARKING



■ **ABSOLUTE MAXIMUM RATING** ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	-500	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	DC	$I_{D(DC)}$	-7	A
	Pulsed (Note 2)	$I_{D(pulse)}$	-14	A
Single Avalanche Energy (Note 3)		E_{AS}	331	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	12.7	V/ns
Power Dissipation ($T_C=25^{\circ}\text{C}$)	TO-220	P_D	85	W
	TO-252		45	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 30\text{mH}$, $I_{AS} = -4.7\text{A}$, $V_{DD} = -50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq -7.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
	TO-252		100	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-220	θ_{JC}	1.47	$^{\circ}\text{C}/\text{W}$
	TO-252		2.77 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

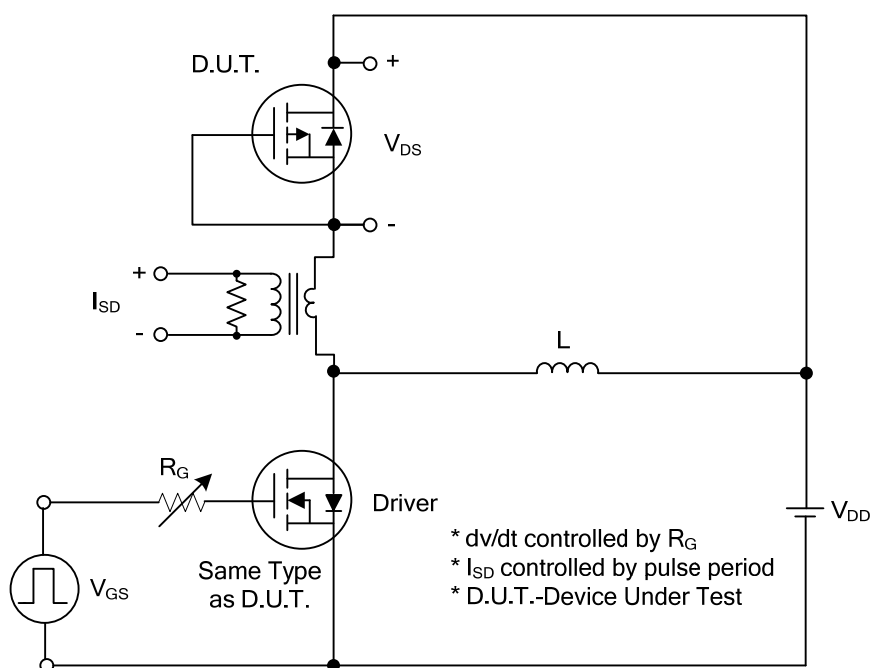
■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =-250μA	-500			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =-500V, V _{GS} =0V			-10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} = V _{GS} , I _D =-250μA	-2.0		-4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =-10V, I _D =-3.5A			1.8	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz		1335		pF
Output Capacitance		C _{OSS}			128		pF
Reverse Transfer Capacitance		C _{RSS}			16		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =-100V, V _{GS} =-10V, I _D =-7.0A , (Note 1, 2)		34.5		nC
Gate to Source Charge		Q _{GS}			8.6		nC
Gate to Drain Charge		Q _{GD}			7.6		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =-100V, V _{GS} =-10V, I _D =-7.0A, R _G =-25Ω (Note 1, 2)		16		ns
Rise Time		t _R			19		ns
Turn-OFF Delay Time		t _{D(OFF)}			127		ns
Fall-Time		t _F			44		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				-7	A
Maximum Body-Diode Pulsed Current		I _{SM}				-14	A
Diode Forward Voltage		V _{SD}	I _F =-7.0A, V _{GS} =0V			-1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _F =-7.0A, V _{GS} =0V, di/dt=100A/μs		280		ns
Body Diode Reverse Recovery Charge		Q _{rr}			6.9		μC

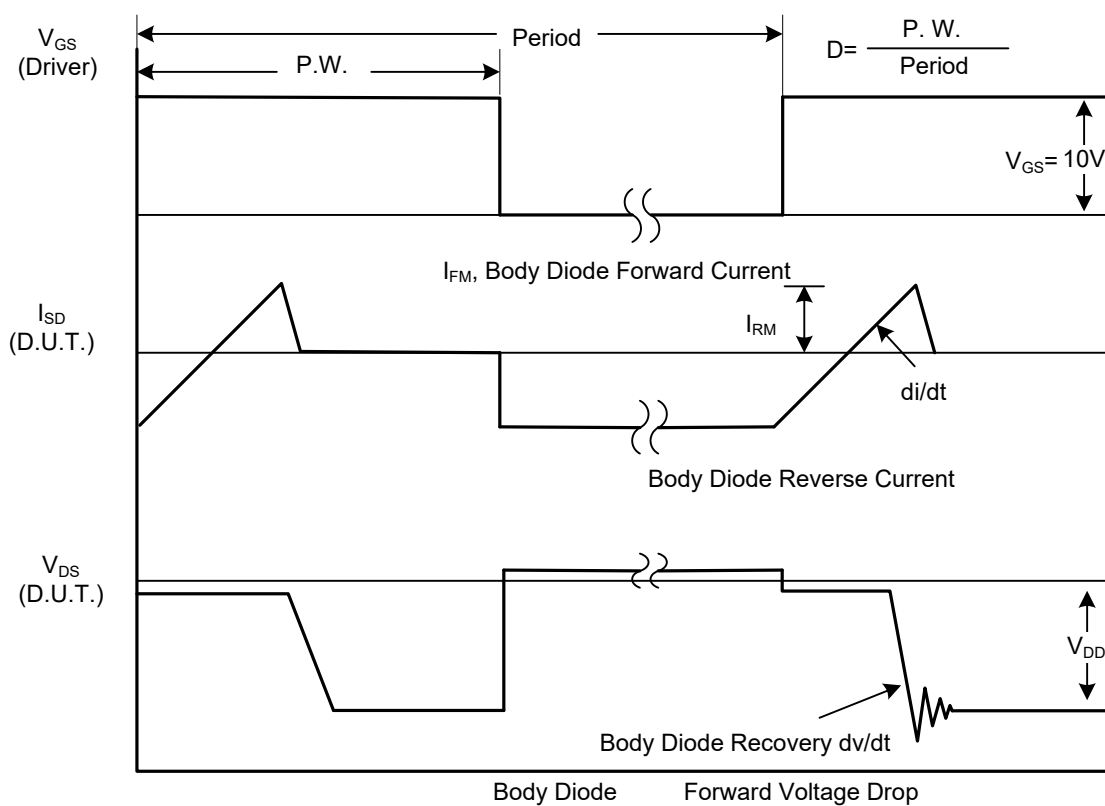
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

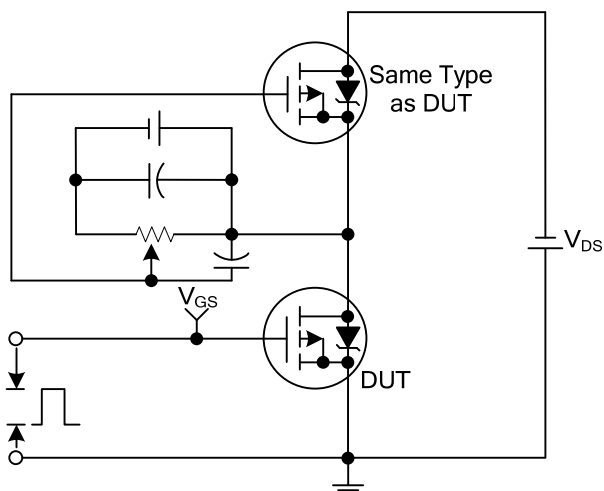


Peak Diode Recovery dv/dt Test Circuit

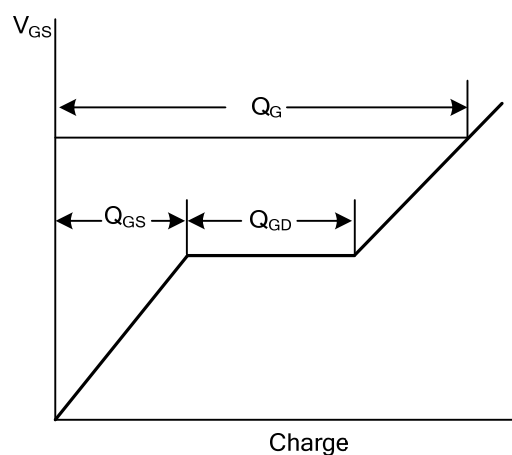


Peak Diode Recovery dv/dt Waveforms

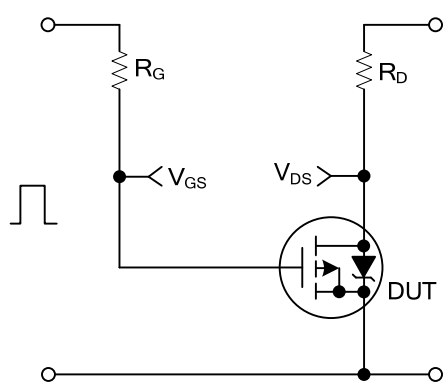
■ TEST CIRCUITS AND WAVEFORMS



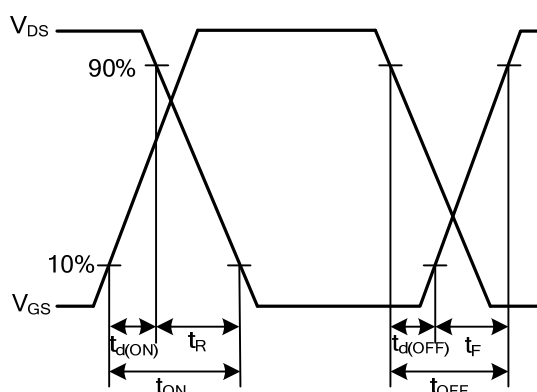
Gate Charge Test Circuit



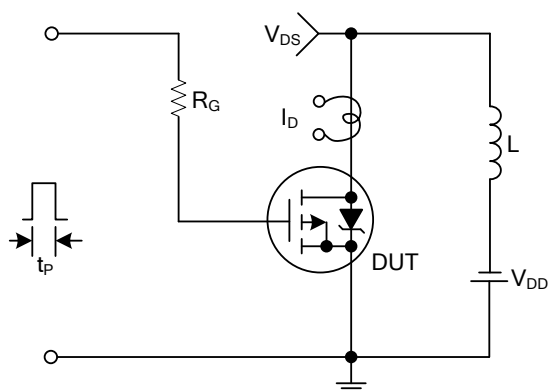
Gate Charge Waveforms



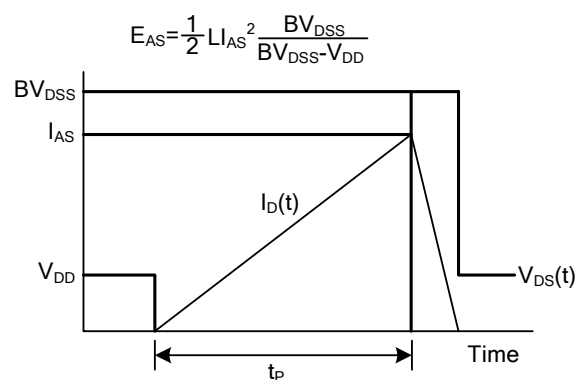
Resistive Switching Test Circuit



Resistive Switching Waveforms

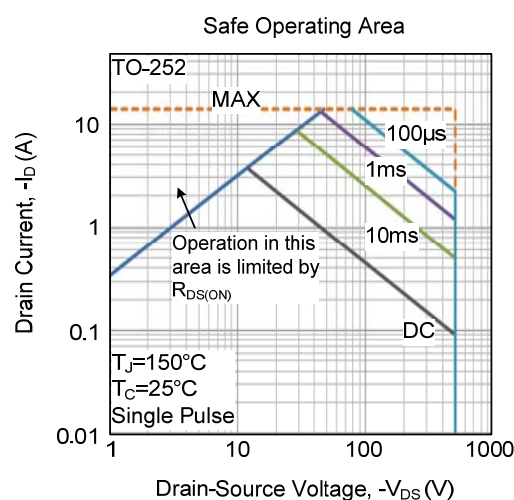
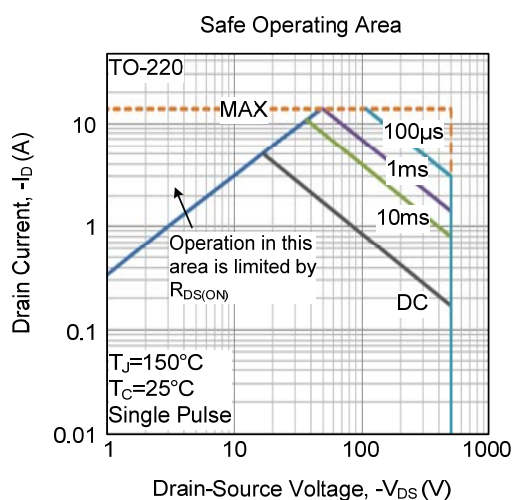


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS



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