

**9N65-ML**

Preliminary

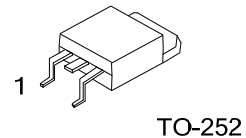
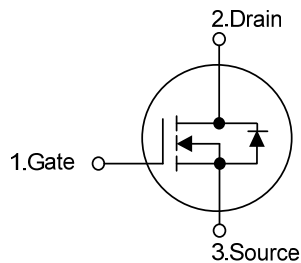
Power MOSFET

**9.0A, 650V N-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **9N65-ML** is a N-Channel enhancement mode silicon gate power MOSFET with Fast Body Diode. is designed high voltage, high speed power switching applications such. such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics.

FEATURES

- * $R_{DS(ON)} \leq 1.3 \Omega$ @ $V_{GS}=10V$, $I_D=4.5A$
- * Fast body diode MOSFET technology
- * Low switching losses due to reduced Q_{rr}
- * Single Pulse Avalanche Energy Rated
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance
- * Avalanche energy tested

SYMBOL

TO-252

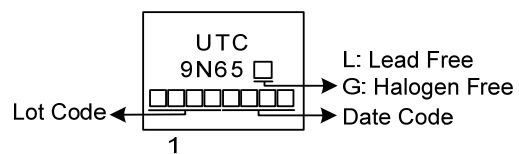
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
9N65L-TN3-R	9N65G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

9N65G-TN3-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	9	A
Pulsed Drain Current (Note 2)	I_{DM}	18	A
Avalanche Energy	E_{AS}	227	mJ
Single Pulsed (Note 3)			
Peak Diode Recovery dv/dt (Note 4)	dv/dt	8.9	V/ns
Power Dissipation	P_D	55	W
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 30\text{mH}$, $I_{AS} = 4.3\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 9.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.27 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

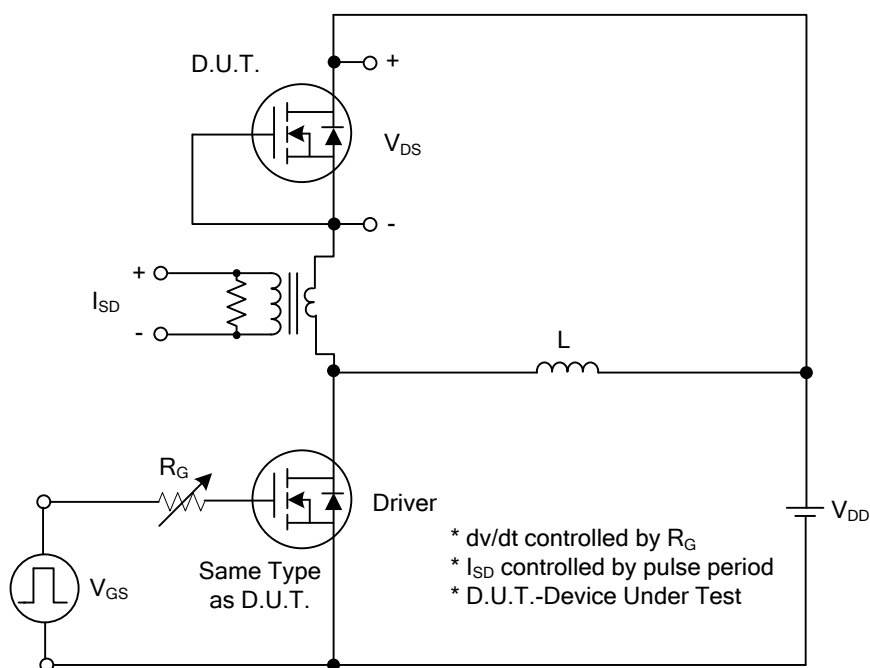
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	650			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =650V, V _{GS} =0V			10	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =30V, V _{DS} =0V			100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =4.5A			1.3	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		1234		pF
Output Capacitance		C _{OSS}			109		pF
Reverse Transfer Capacitance		C _{RSS}			8		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =520V, V _{GS} =10V, I _D =9.0A I _G =1mA (Note 1, 2)		31		nC
Gate-Source Charge		Q _{GS}			9		nC
Gate-Drain Charge		Q _{GD}			8		nC
Turn-On Delay Time (Note 1)		t _{D(ON)}	V _{DS} =100V, V _{GS} =10V, I _D =9.0A R _G =25Ω (Note 1, 2)		13		Ns
Turn-On Rise Time		t _R			18		Ns
Turn-Off Delay Time		t _{D(OFF)}			90		Ns
Turn-Off Fall Time		t _F			39		Ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
Maximum Body-Diode Continuous Current		I _S				9	A
Maximum Body-Diode Pulsed Current		I _{SM}				18	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =9.0A , V _{GS} =0V			1.4	V

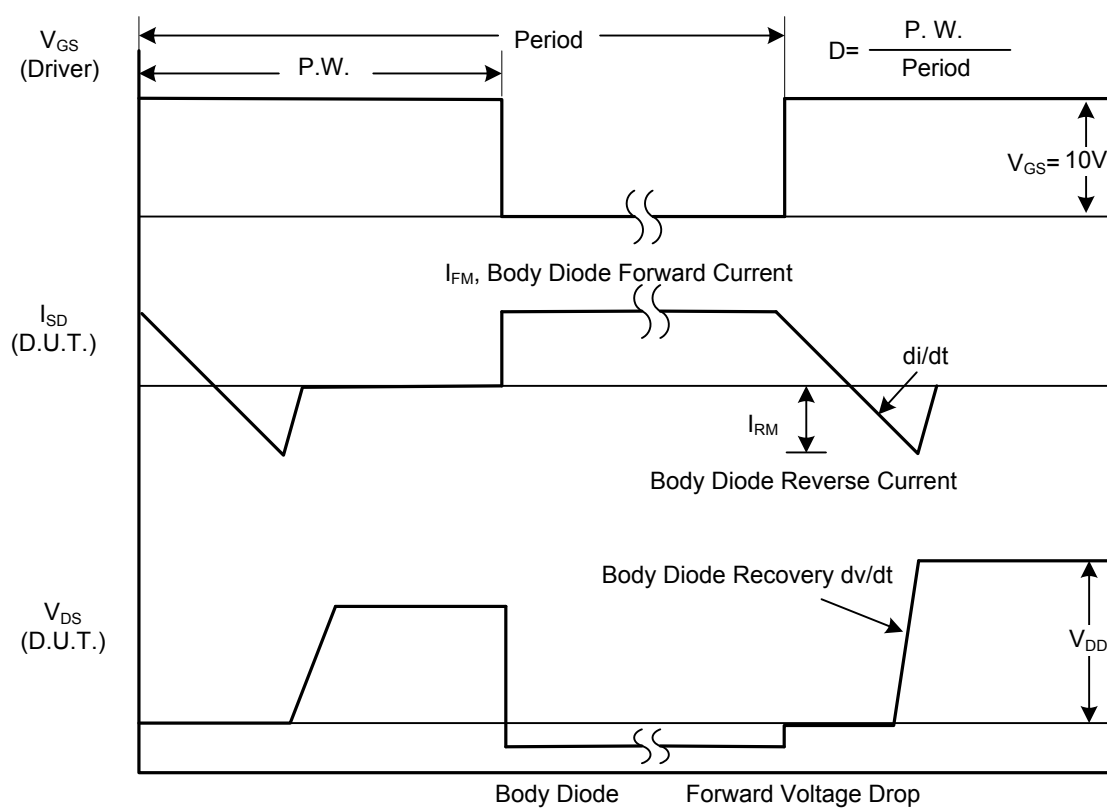
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

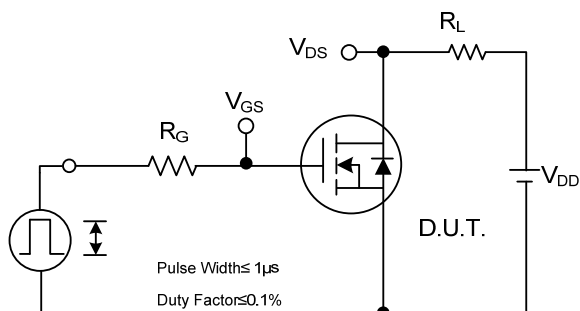


Peak Diode Recovery dv/dt Test Circuit

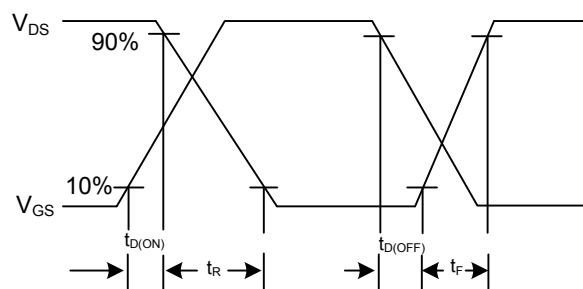


Peak Diode Recovery dv/dt Waveforms

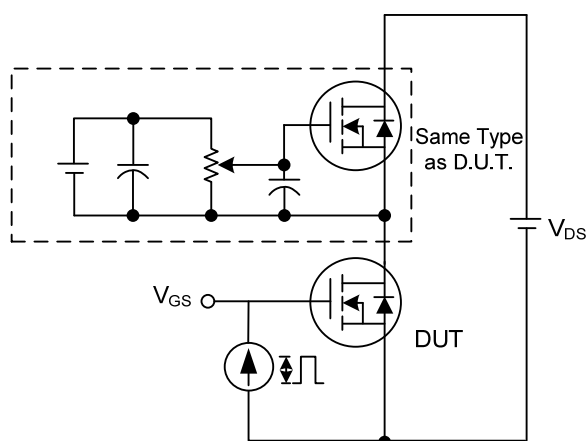
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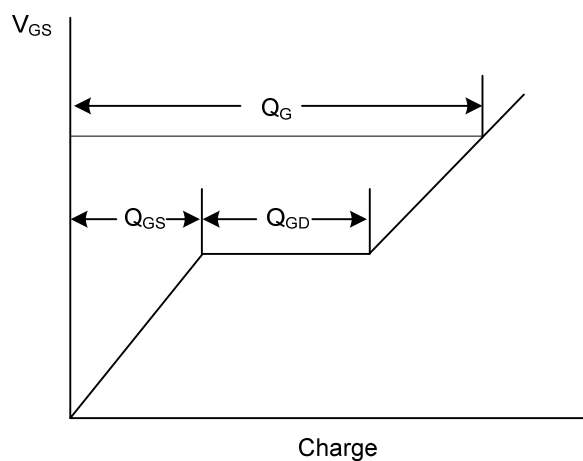
Switching Test Circuit



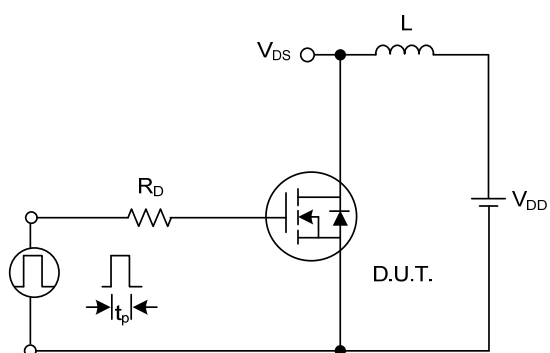
Switching Waveforms



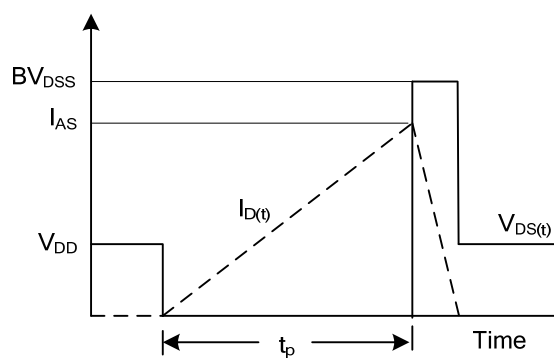
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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