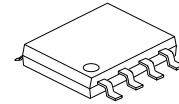


**F2NN50-LC1**

Preliminary

*Power MOSFET***2.0A, 500V DUAL N-CHANNEL
ENHANCEMENT MODE POWER
MOSFET****■ DESCRIPTION**

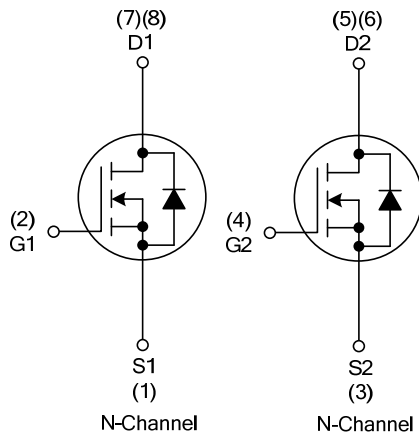
The UTC **F2NN50-LC1** is a dual N-Channel enhancement mode silicon gate power MOSFET with Fast Body Diode, is designed high voltage, high speed power switching applications such, is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient AC to DC converters and bridge circuits.



SOP-8

■ FEATURES

- * $R_{DS(ON)} \leq 5.0 \Omega$ @ $V_{GS}=10V$, $I_D=1.0A$
- * Fast body diode MOSFET technology
- * Fast Switching Speed
- * Simple Drive Requirement

■ SYMBOL

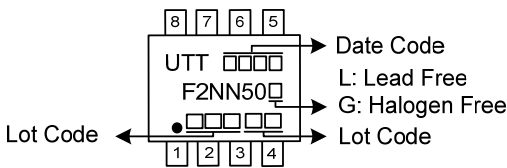
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
F2NN50L-S08-R	F2NN50G-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: S: Source G: Gate D: Drain

F2NN50G-S08-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	500	V
Gate-Source Voltage		V _{GSS}	±30	V
Drain Current	Continuous	I _D	2	A
	Pulsed (Note 2)	I _{DM}	4	A
Avalanche Energy	Single Pulsed (Note 3)	E _{AS}	63	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	6.6	V/ns
Power Dissipation		P _D	1.95	W
Junction Temperature		T _J	+150	°C
Storage Temperature		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L = 30mH, I_{AS} = 2.0A, V_{DD} = 50V, R_G = 25 Ω Starting T_J = 25°C

4. I_{SD} ≤ 2.0A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ _{JA}	90	°C/W
Junction to Case		θ _{JC}	65	°C/W

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

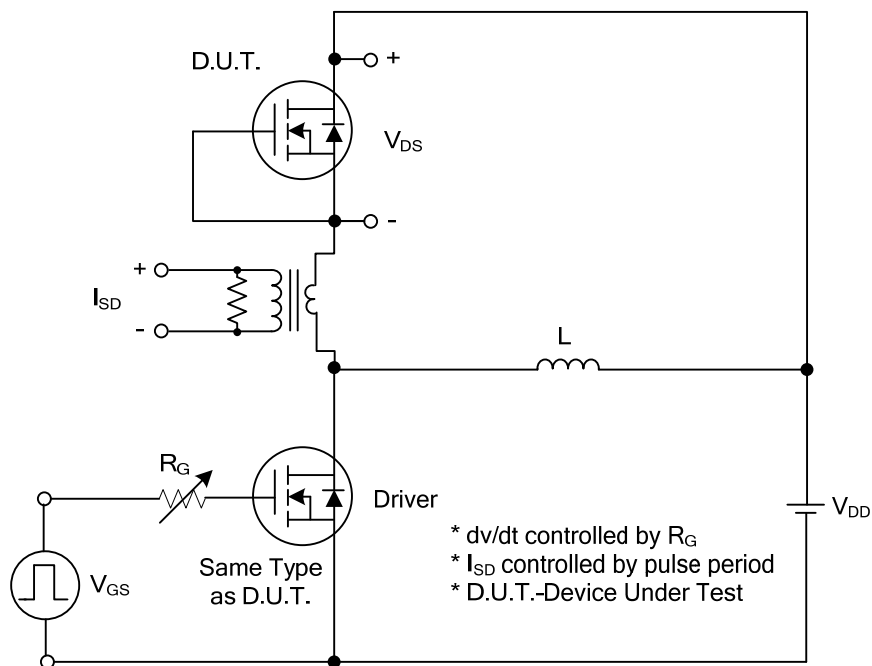
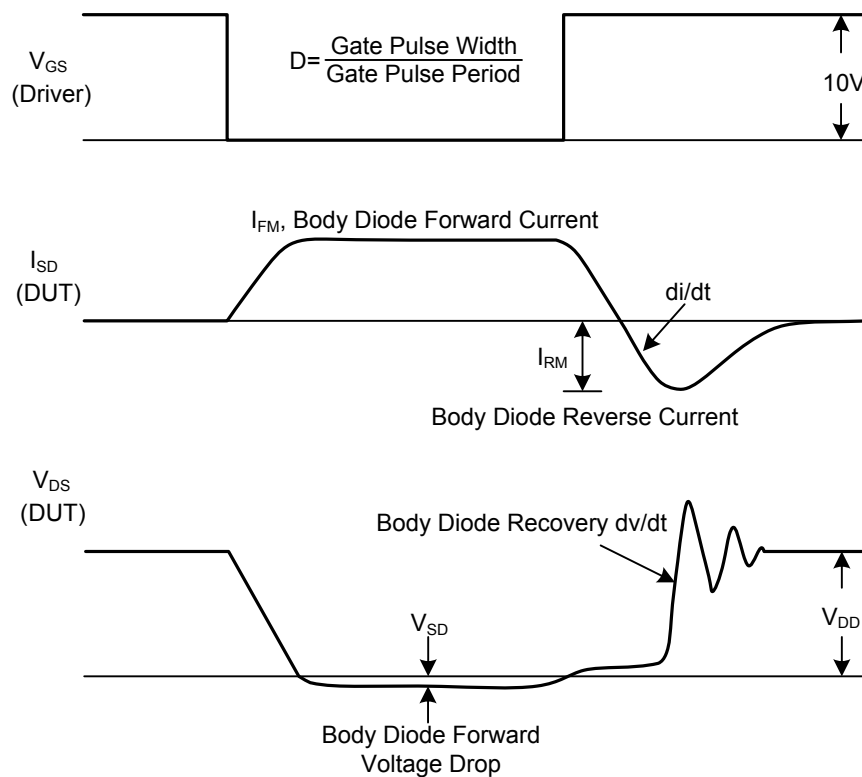
■ ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D = 250μA	500			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =500V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =30V, V _{DS} =0V			100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =1.0A			5.0	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0 MHz		232		pF
Output Capacitance		C _{OSS}			31		pF
Reverse Transfer Capacitance		C _{RSS}			3.6		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =400V, V _{GS} =10V, I _D =2.0A I _G =1mA (Note 1, 2)		11.3		nC
Gateource Charge		Q _{GS}			4		nC
Gate-Drain Charge		Q _{GD}			1.5		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =100V, V _{GS} =10V, I _D =2.0A, R _G =25Ω (Note 1, 2)		5		ns
Rise Time		t _R			16		ns
Turn-off Delay Time		t _{D(OFF)}			20		ns
Fall-Time		t _F			25		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				2	A
Maximum Body-Diode Pulsed Current		I _{SM}				4	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =2.0A , V _{GS} =0V			1.4	V
Reverse Recovery Time (Note 1)		t _{rr}	I _S =2.0A , V _{GS} =0V		65		ns
Reverse Recovery Charge		Q _{rr}	di/dt=100A/μs (Note1)		215		nC

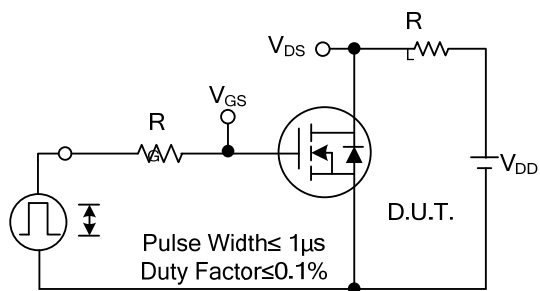
Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

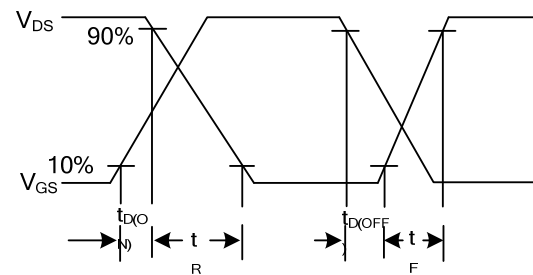
■ TEST CIRCUITS AND WAVEFORMS

Peak Diode Recovery dv/dt Test CircuitPeak Diode Recovery dv/dt Waveforms

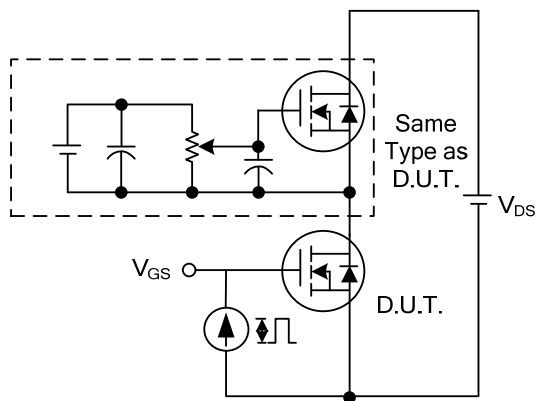
■ TEST CIRCUITS AND WAVEFORMS



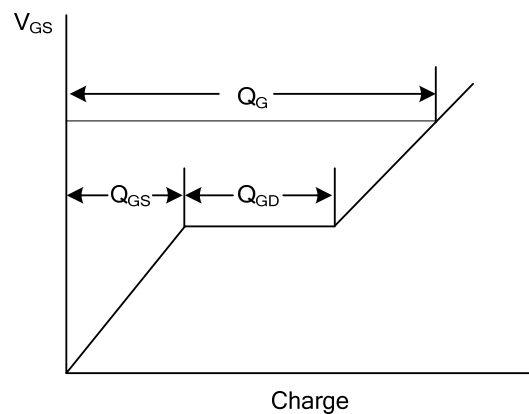
Switching Test Circuit



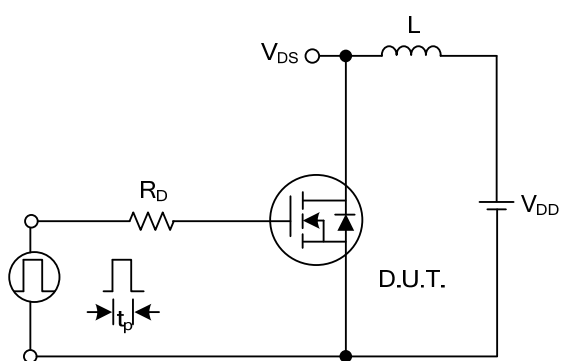
Switching Waveforms



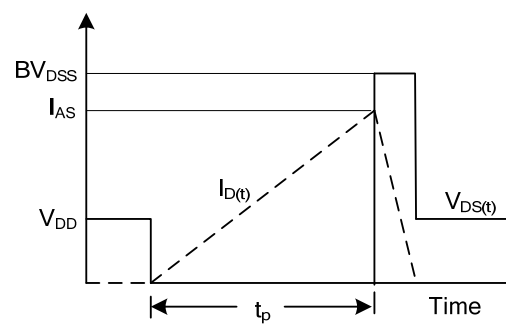
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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