

**F7N50-SE1**

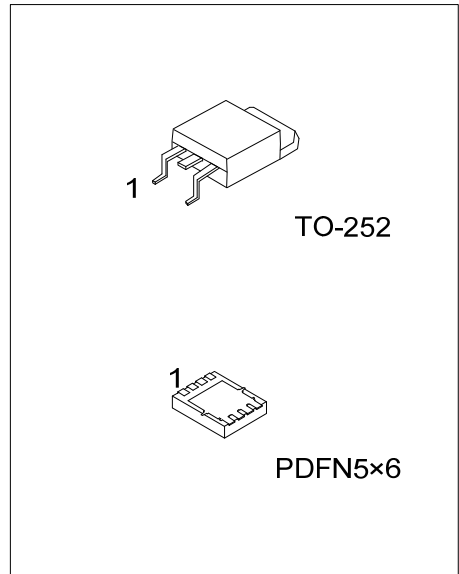
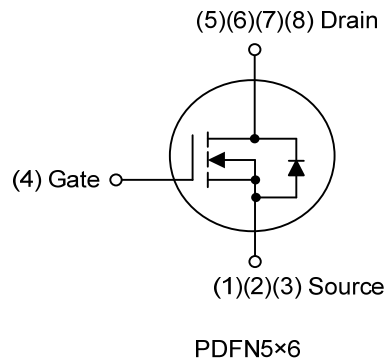
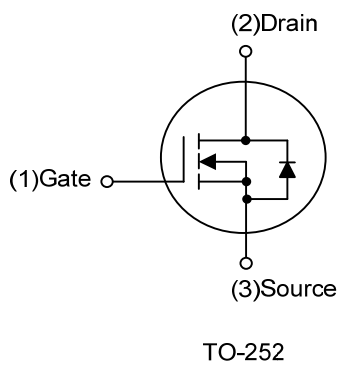
Preliminary

POWER MOSFET**7.0A, 500V N-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **F7N50-SE2** is an N-Channel power MOSFET. is designed high voltage, high speed power switching applications such. such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics.

FEATURES

- * $R_{DS(ON)} \leq 1.6 \Omega$ @ $V_{GS}=10V$, $I_D=3.5A$
- * Fast Switching Speeds
- * 100% avalanche tested
- * Linear Transfer Characteristics
- * High Input Impedance

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
F7N50L-SE1-TN3-R	F7N50G-SE1-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
F7N50L-SE1-P5060-R	F7N50G-SE1-P5060-R	PDFN5x6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

F7N50G-SE1-TN3-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) TN3: TO-252, P5060: PDFN5x6
		(3) Version Code	(3) Version SE2
		(4) Green Package	(4) G: Halogen Free and Lead Free, L: Lead Free

MARKING

TO-252	PDFN5×6
UTC F7N50 SE1 1 Version Code Lot Code L: Lead Free G: Halogen Free Date Code	UTC F7N50 SE1 • Version Code Lot Code Date Code

■ **ABSOLUTE MAXIMUM RATING** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	DC	I_D	7	A
	Pulsed (Note 2)	I_{DM}	14	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	90	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	7.6	V/ns
Power Dissipation	TO-252	P_D	50	W
	PDFN5x6		36	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 10\text{mH}$, $I_{AS} = 4.2\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$ Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 7.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
	PDFN5x6		65 (Note)	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-252	θ_{JC}	2.5 (Note)	$^{\circ}\text{C}/\text{W}$
	PDFN5x6		3.47 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

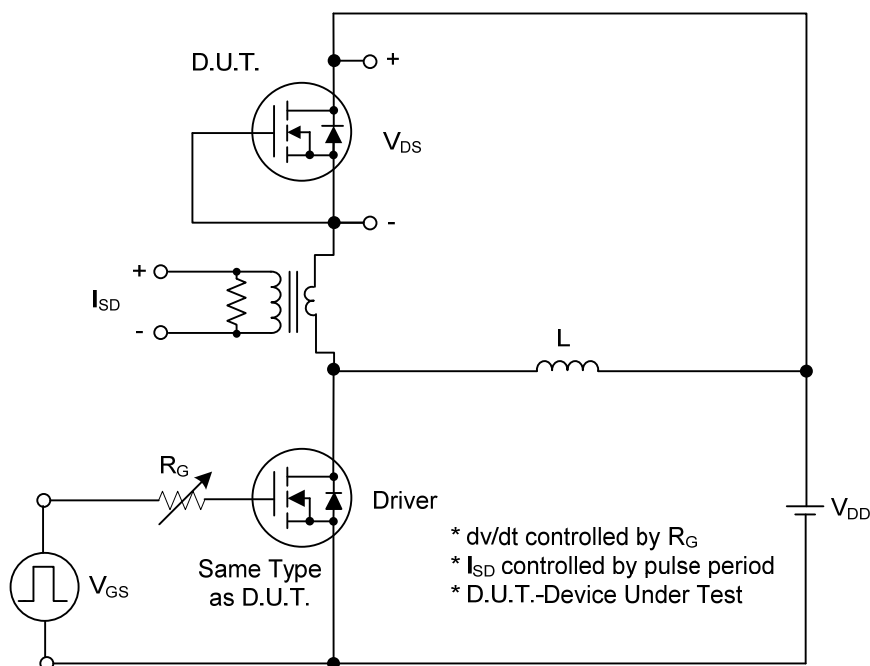
■ ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	500			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =500V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =3.5A			1.6	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		674		pF
Output Capacitance		C _{OSS}			65		pF
Reverse Transfer Capacitance		C _{RSS}			3		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =400V, V _{GS} =10V, I _D =7.0A (Note 1, 2)		21		nC
Gate to Source Charge		Q _{GS}			5		nC
Gate to Drain Charge		Q _{GD}			2		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =7.0A, R _G =25Ω (Note 1, 2)		8		ns
Rise Time		t _R			18		ns
Turn-OFF Delay Time		t _{D(OFF)}			38		ns
Fall-Time		t _F			22		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				7	A
Diode Forward Voltage		V _{SD}	I _F =7.0A, V _{GS} =0V			1.4	V
Reverse Recovery Time		t _{rr}	I _S =7.0A, V _{GS} =0V,		108		ns
Reverse Recovery Charge (Note 1)		Q _{rr}	dI _F /dt = 100 A/μs		332		nC

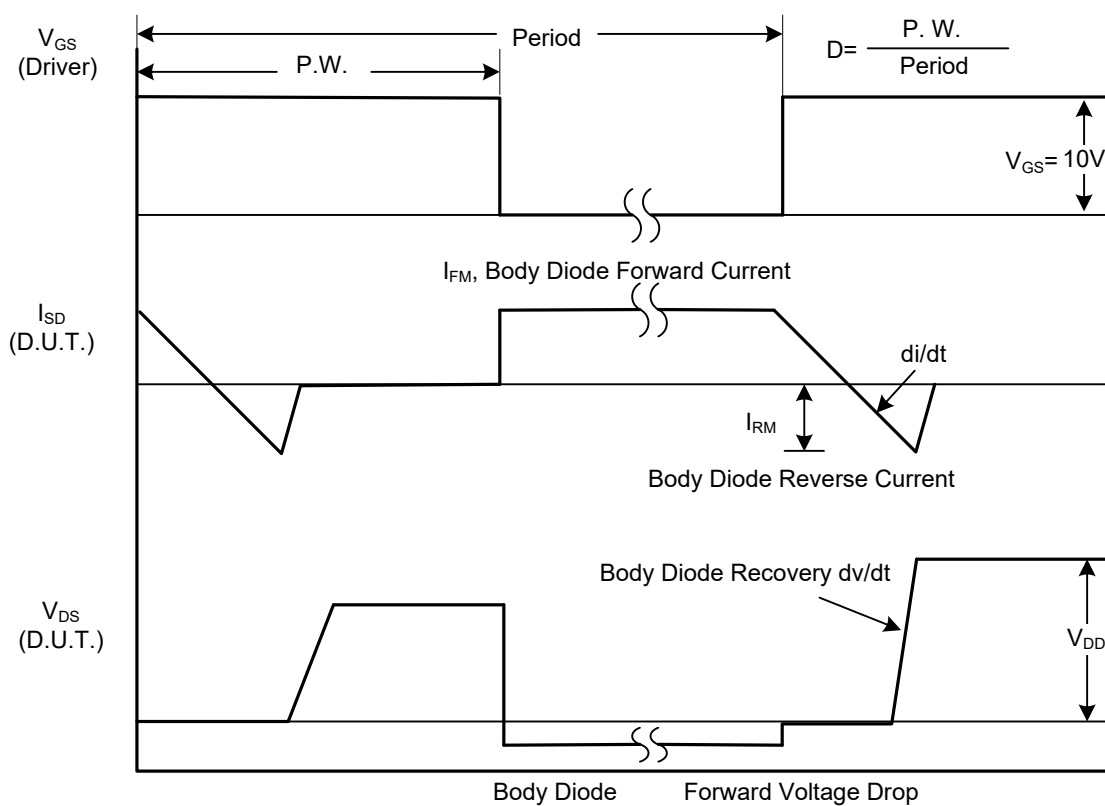
Notes: 1. Pulse Test: Pulse width ≤ 500μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

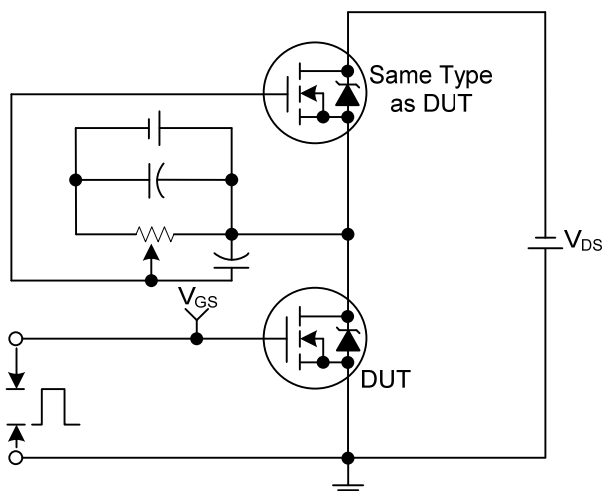


Peak Diode Recovery dv/dt Test Circuit

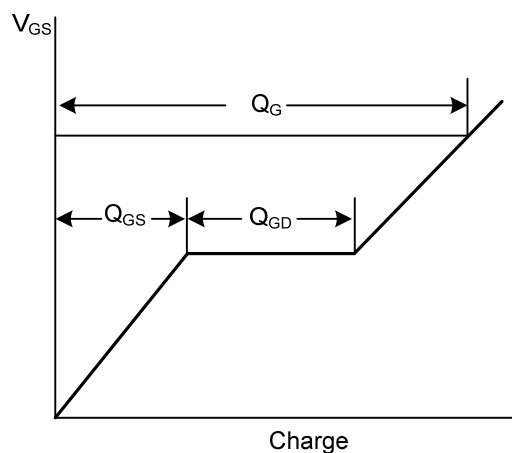


Peak Diode Recovery dv/dt Waveforms

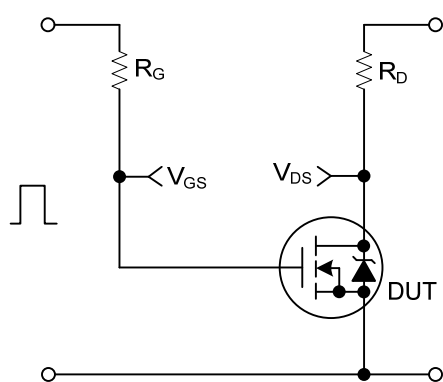
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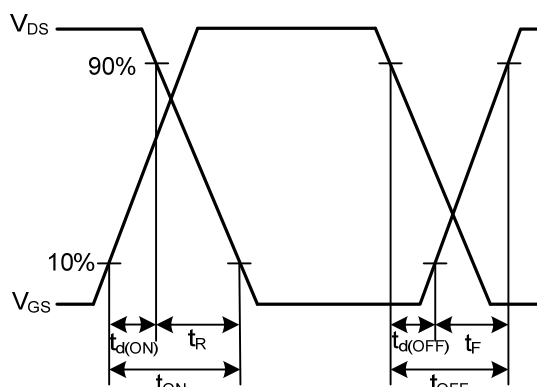
Gate Charge Test Circuit



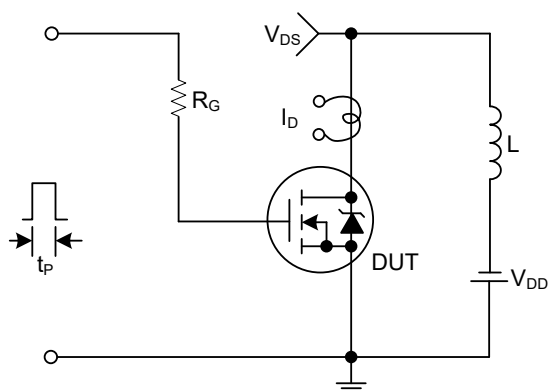
Gate Charge Waveforms



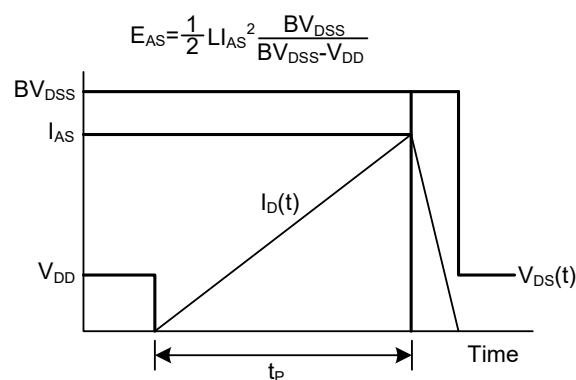
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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