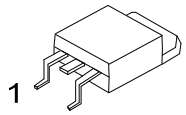
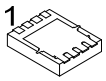
# F7N50-SE1

**Preliminary** | ***POWER MOSFET***

## 7.0A, 500V N-CHANNEL POWER MOSFET




TO-252




PDFN5×6

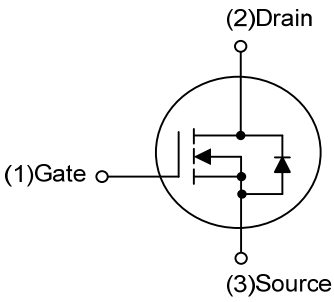
### ■ DESCRIPTION

The UTC **F7N50-SE2** is an N-Channel power MOSFET. is designed high voltage, high speed power switching applications such. such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics.

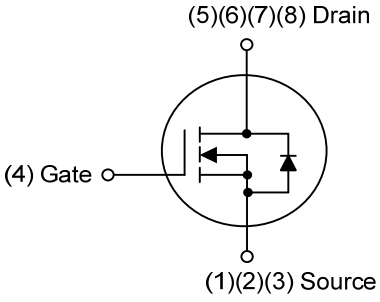
### ■ FEATURES

* $R_{DS(ON)} \leq 1.6\ \Omega$ @ $V_{GS}$=10V, $I_D$=3.5A
* Fast Switching Speeds
* 100% avalanche tested
* Linear Transfer Characteristics
* High Input Impedance

### ■ SYMBOL




TO-252




PDFN5×6

### ■ ORDERING INFORMATION

| Ordering Number | | Package | Pin Assignment | | | | | | | | Packing |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Lead Free | Halogen Free | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
| F7N50L-SE1-TN3-R | F7N50G-SE1-TN3-R | TO-252 | G | D | S | - | - | - | - | - | Tape Reel |
| F7N50L-SE1-P5060-R | F7N50G-SE1-P5060-R | PDFN5×6 | S | S | S | G | D | D | D | D | Tape Reel |

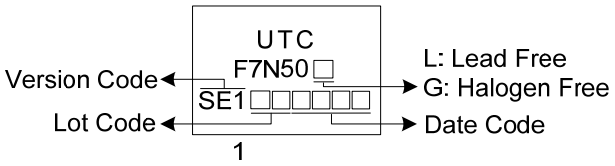
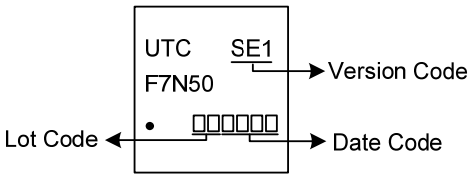
Note: Pin Assignment: G: Gate D: Drain S: Source

F7N50G-SE1-TN3-R

(1)Packing Type
(2)Package Type
(3)Version Code
(4)Green Package

(1) R: Tape Reel
(2) TN3: TO-252, P5060: PDFN5×6
(3) Version SE2
(4) G: Halogen Free and Lead Free, L: Lead Free

## ■ MARKING

| TO-252 | PDFN5×6 |
|---|---|
|  |  |

## ■ ABSOLUTE MAXIMUM RATING ($T_C$=25°C, unless otherwise specified)

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | 500 | V |
| Gate-Source Voltage | | $V_{GSS}$ | ±30 | V |
| Drain Current | DC | $I_D$ | 7 | A |
| | Pulsed (Note 2) | $I_{DM}$ | 14 | A |
| Avalanche Energy | Single Pulsed (Note 3) | $E_{AS}$ | 90 | mJ |
| Peak Diode Recovery dv/dt (Note 4) | | dv/dt | 7.6 | V/ns |
| Power Dissipation | TO-252 | $P_D$ | 50 | W |
| | PDFN5x6 | | 36 | W |
| Junction Temperature | | $T_J$ | +150 | °C |
| Storage Temperature Range | | $T_{STG}$ | -55 ~ +150 | °C |

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L = 10mH, $I_{AS}$ = 4.2A, $V_{DD}$ = 50V, $R_G$ = 25Ω Starting $T_J$ = 25°C
4. $I_{SD}$ ≤ 7.0A, di/dt ≤ 200A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C

## ■ THERMAL DATA

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Junction to Ambient | TO-252 | $\theta_{JA}$ | 110 | °C/W |
| | PDFN5×6 | | 65 Note) | °C/W |
| Junction to Case | TO-252 | $\theta_{JC}$ | 2.5 (Note) | °C/W |
| | PDFN5×6 | | 3.47 (Note) | °C/W |

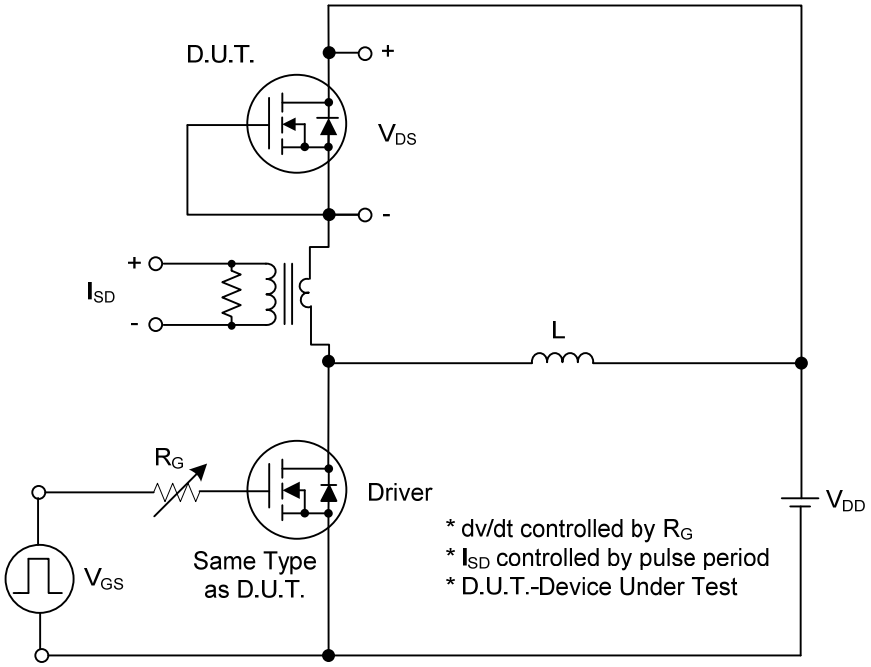
Note: Device mounted on FR-4 substrate $P_C$ board, 2oz copper, with 1inch square copper plate.

## ■ ELECTRICAL CHARACTERISTICS ($T_J$=25°C unless otherwise specified)

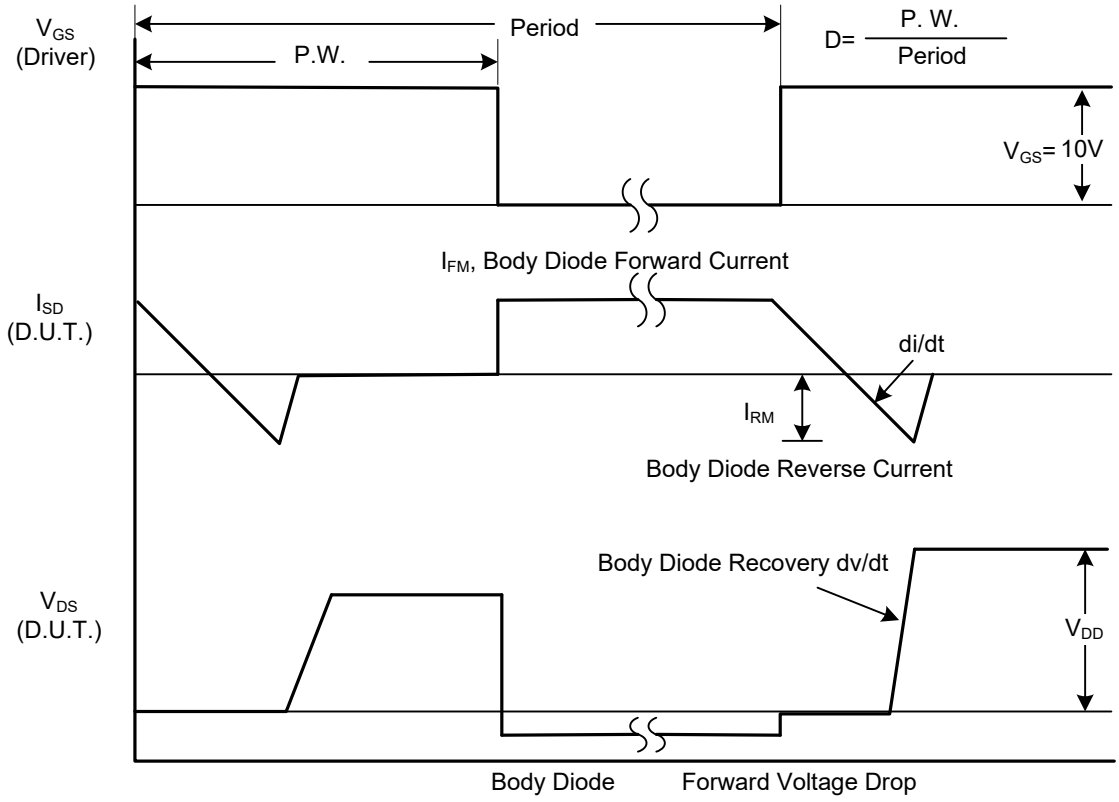
| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain-Source Breakdown Voltage | | $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=250μA | 500 | | | V |
| Drain-Source Leakage Current | | $I_{DSS}$ | $V_{DS}$=500V, $V_{GS}$=0V | | | 10 | μA |
| Gate-Source Leakage Current | Forward | $I_{GSS}$ | $V_{GS}$=+30V, $V_{DS}$=0V | | | +100 | nA |
| | Reverse | | $V_{GS}$=-30V, $V_{DS}$=0V | | | -100 | nA |
| **ON CHARACTERISTICS** | | | | | | | |
| Gate Threshold Voltage | | $V_{GS(TH)}$ | $V_{DS}$=$V_{GS}$, $I_D$=250μA | 2.0 | | 4.0 | V |
| Static Drain-Source On-State Resistance | | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=3.5A | | | 1.6 | Ω |
| **DYNAMIC PARAMETERS** | | | | | | | |
| Input Capacitance | | $C_{ISS}$ | $V_{GS}$=0V, $V_{DS}$=25V, f=1.0MHz | | 674 | | pF |
| Output Capacitance | | $C_{OSS}$ | | | 65 | | pF |
| Reverse Transfer Capacitance | | $C_{RSS}$ | | | 3 | | pF |
| **SWITCHING PARAMETERS** | | | | | | | |
| Total Gate Charge | | $Q_G$ | $V_{DS}$=400V, $V_{GS}$=10V, $I_D$=7.0A (Note 1, 2) | | 21 | | nC |
| Gate to Source Charge | | $Q_{GS}$ | | | 5 | | nC |
| Gate to Drain Charge | | $Q_{GD}$ | | | 2 | | nC |
| Turn-ON Delay Time | | $t_{D(ON)}$ | $V_{DD}$=100V, $V_{GS}$=10V, $I_D$=7.0A, $R_G$=25Ω (Note 1, 2) | | 8 | | ns |
| Rise Time | | $t_R$ | | | 18 | | ns |
| Turn-OFF Delay Time | | $t_{D(OFF)}$ | | | 38 | | ns |
| Fall-Time | | $t_F$ | | | 22 | | ns |
| **SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS** | | | | | | | |
| Maximum Continuous Drain-Source Diode Forward Current | | $I_S$ | | | | 7 | A |
| Diode Forward Voltage | | $V_{SD}$ | $I_F$=7.0A, $V_{GS}$=0V | | | 1.4 | V |
| Reverse Recovery Time | | $t_{rr}$ | $I_S$=7.0A, $V_{GS}$=0V, $dI_F/dt$ = 100 A/μs | | 108 | | ns |
| Reverse Recovery Charge (Note 1) | | $Q_{rr}$ | | | 332 | | nC |

Notes: 1. Pulse Test: Pulse width ≤ 500μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

## ■ TEST CIRCUITS AND WAVEFORMS

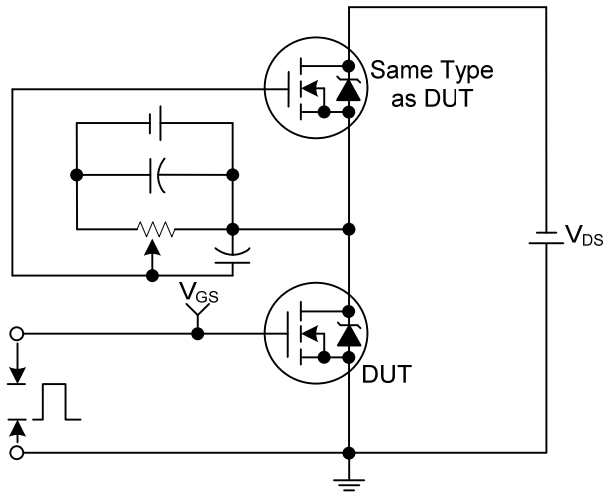



**Peak Diode Recovery dv/dt Test Circuit**

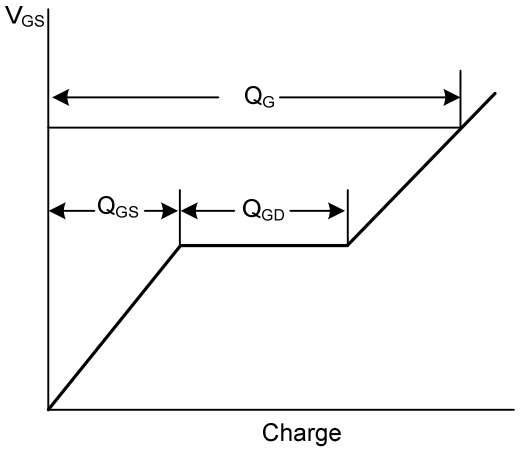



**Peak Diode Recovery dv/dt Waveforms**

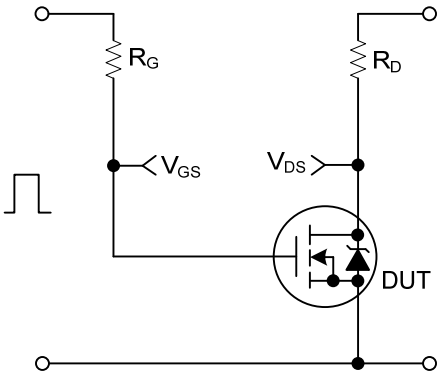
## ■ TEST CIRCUITS AND WAVEFORMS



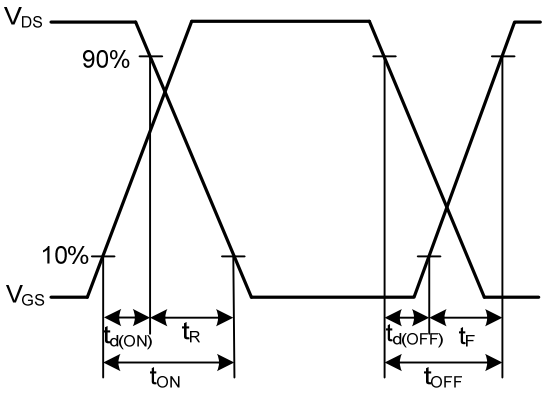

Gate Charge Test Circuit



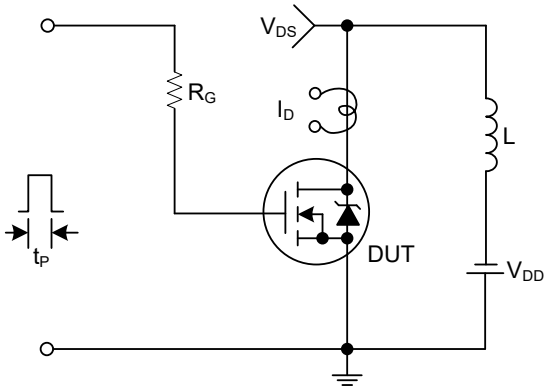

Gate Charge Waveforms



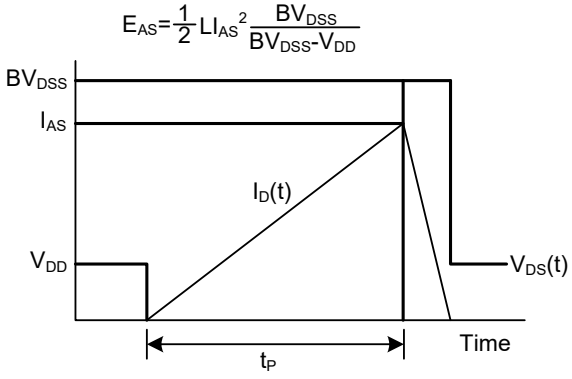

Resistive Switching Test Circuit




Resistive Switching Waveforms




Unclamped Inductive Switching Test Circuit




Unclamped Inductive Switching Waveforms