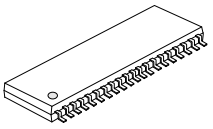
PPHDMI2020 **Preliminary** ***TVS DIODE***

HDMI TRANSMITTER PORT PROTECTION AND INTERFACE DEVICE



SSOP-40

■ DESCRIPTION

The UTC **PPHDMI2020** HDMI Transmitter Port Protection and Interface device is specifically designed for next generation HDMI source interface protection.

An integrated package provides all ESD, level shift, overcurrent output protection and backdrive protection for an HDMI port in a single SSOP-40 package.

The UTC **PPHDMI2020** also incorporates a silicon overcurrent protection device for +5V supply voltage output to the connector.

■ FEATURES

* 0.05pF matching capacitance between the TMDS intra-pair
* HDMI 1.3 compliant
* Level shifting/isolation circuitry
* Provides ESD protection to IEC61000-4-2 Level 4
  - 8kV contact discharge
  - 15kV air discharge
* Backdrive protection
* Overcurrent output protection
* Simplified layout for HDMI connectors

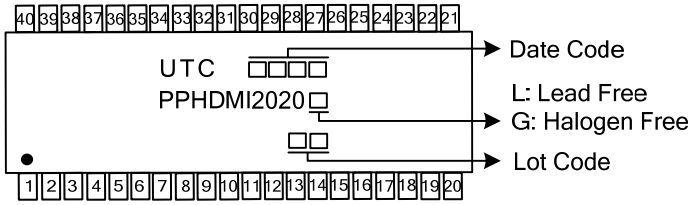
■ ORDERING INFORMATION

Order Number		Package	Packing
Lead Free	Halogen Free		
PPHDMI2020L-R40-R	PPHDMI2020G-R40-R	SSOP-40	Tape Reel

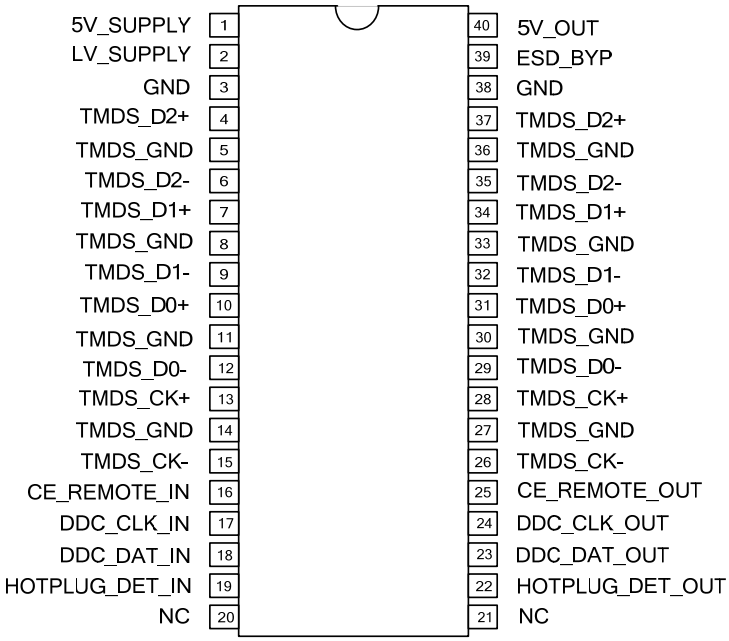
PPHDMI2020G-R40-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) R40: SSOP-40
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

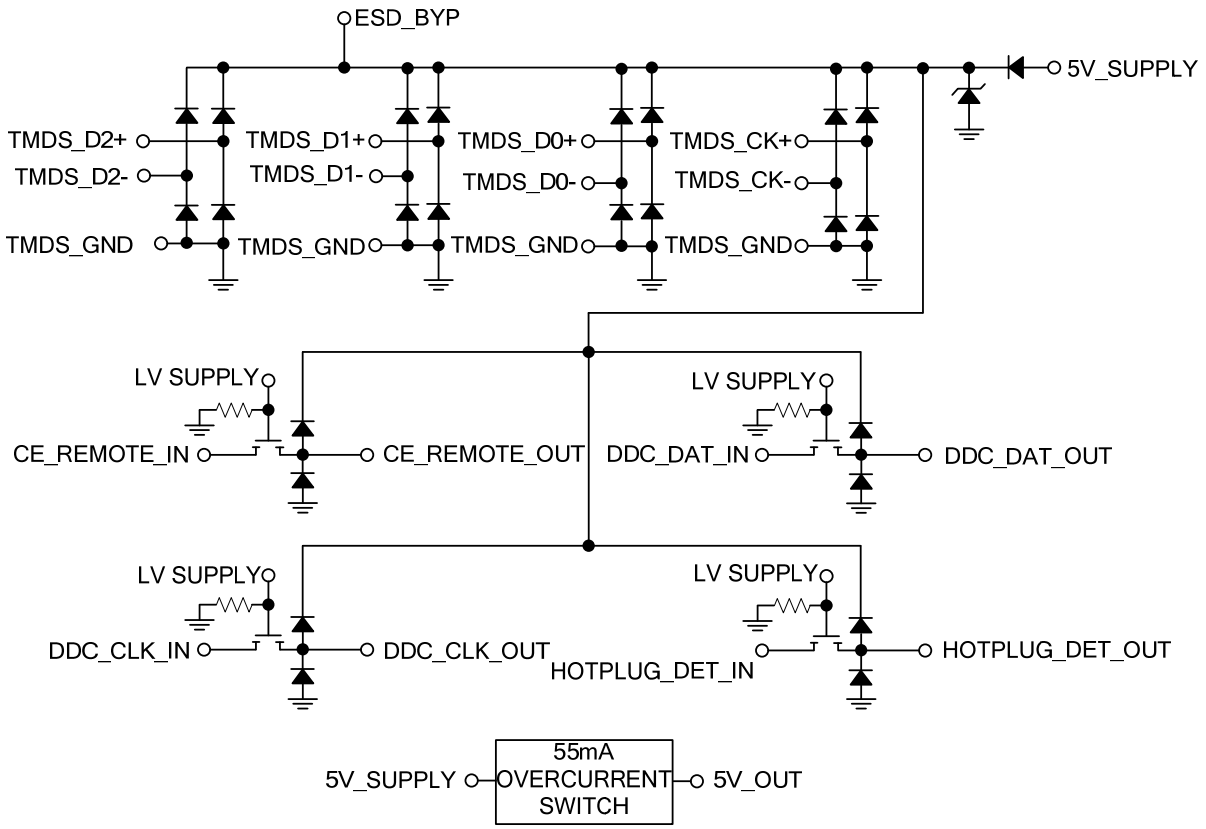
PIN NO.	PIN NAME	DESCRIPTION
1	5V_SUPPLY	Current source for 5V_OUT.
2	LV_SUPPLY	Bias for CE / DDC / HOTPLUG level shifters.
3, 38	GND	Supply GND reference.
4, 37	TMDS_D2+	TMDS 0.9pF ESD protection (Note 1).
5, 8, 11, 14, 27, 30, 33, 36	TMDS_GND	TMDS ESD and Parasitic GND return. (Note 3)
6, 35	TMDS_D2-	TMDS 0.9pF ESD protection. (Note 1)
7, 34	TMDS_D1+	TMDS 0.9pF ESD protection. (Note 1)
9, 32	TMDS_D1-	TMDS 0.9pF ESD protection. (Note 1)
10, 31	TMDS_D0+	TMDS 0.9pF ESD protection. (Note 1)
12, 29	TMDS_D0-	TMDS 0.9pF ESD protection. (Note 1)
13, 28	TMDS_CK+	TMDS 0.9pF ESD protection. (Note 1)
15, 26	TMDS_CK-	TMDS 0.9pF ESD protection. (Note 1)
16	CE_REMOTE_IN	LV_SUPPLY referenced logic level into ASIC.
17	DDC_CLK_IN	LV_SUPPLY referenced logic level into ASIC.
18	DDC_DAT_IN	LV_SUPPLY referenced logic level into ASIC.
19	HOTPLUG_DET_IN	LV_SUPPLY referenced logic level into ASIC.
20, 21	NC	
22	HOTPLUG_DET_OUT	5V_SUPPLY referenced logic level out plus 3.5pF ESD (Note 2) to connector
23	DDC_DAT_OUT	5V_SUPPLY referenced logic level out plus 3.5pF ESD to connector.
24	DDC_CLK_OUT	5V_SUPPLY referenced logic level out plus 3.5pF ESD to connector.
25	CE_REMOTE_OUT	5V_SUPPLY referenced logic level out plus 3.5pF ESD to connector.
39	ESD_BYP	This pin must be connected to a 0.1μF ceramic capacitor.
40	5V_OUT	55mA minimum overcurrent protected 5V output. This output must be bypassed with a 0.1μF ceramic capacitor

Noets: 1. These 2 pins need to be connected together in-line on the PCB.

2. This output can be connected to an external 0.1μF ceramic capacitor, resulting in an increased ESD withstand voltage rating.

3.These pins should be routed directly to the associated GND pins on the HDMI connector with single point ground vias at the connector.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
V_{CC5V}, V_{CCLV}		6.0	V
DC Voltage at any Channel Input		6.0	V
Storage Temperature	T_{STG}	-65~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ STANDARD (RECOMMENDED) OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating Supply Voltage	5V_SUPPLY	GND	5	5.5	V
Bias Supply Voltage	LV_SUPPLY	1	3.3	5.5	V
Operating Temperature Range	T_{OTR}	-40		85	°C

■ ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Current		I_{CC5V}	5V_SUPPLY=5.0V		110	130	μA
Bias Supply Current		I_{CCLV}	LV_SUPPLY=3.3V		1	5	μA
5V_OUT Overcurrent Output Drop		V_{DROP}	5V_SUPPLY=5.0V, I_{OUT}=55mA		65	100	mV
5V_OUT Short Circuit Current Limit		I_{SC}	5V_SUPPLY=5.0V, 5V_OUT=GND	90	135	175	mA
OFF State Leakage Current, Level Shifting NFET		I_{OFF}	LV_SUPPLY 0V		0.1	5	μA
Current Conducted from Output Pins to V_SUPPLY Rails When Powered Down		$I_{BACKDRIVE}$	5V_SUPPLY V_{CH_OUT}; Signal pins: TMDS_D[2:0]+/-, TMDS_CK+/-, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT, 5V_OUT Only		0.1	5	μA
Current Through CE-REMOTE_OUT When Powered Down		$I_{BACKDRIVE}$, CEC	CE-REMOTE_IN = LV_SUPPLY< CE_REMOTE_OUT		0.1	1	μA
VOLTAGE Drop Across Level Shifting NFET When ON		V_{ON}	LV_SUPPLY=2.5V, V_S=GND, I_{DS}=3mA	75	95	140	mV
Diode Forward Voltage	Top Diode	V_F	I_F=8mA, T_A=25°C	0.6	0.85	0.95	V
	Bottom Diode			0.6	0.85	0.95	V
ESD Withstand Voltage, Contact Discharge Per IEC 61000-4-2 Standard (IEC)		V_{ESD}	Pins 4, 7, 10, 13, 22, 23, 24, 25, 26, 29, 32, 35, 40; T_A=25°C (Note 2)	±8			kV
Channel Clamp Voltage	Positive Transients	V_{CL}	T_A=25°C, I_{PP}=1A, t_P=8/20μS; (Note 3)		10.8		V
	Negative Transients				-2.1		V
Dynamic Resistance	Positive Transients	R_{DYN}	I_{PP}=1A, t_P=8/20μS; T_A=25°C; (Note 3)		1.4		Ω
	Negative Transients				0.9		Ω

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TMDS Channel Leakage Current	ILEAK	T_A=25°C		0.01	1	μA
TMDS Channel Input Capacitance	CIN, TMDS	5V_SUPPLY=5.0V, Measured at 1MHz, VBIAS=2.5V		0.9	1.2	pF
TMDS Channel Input Capacitance Matching	ΔCIN, TMDS	5V_SUPPLY= 5.0V, Measured at 1MHz, VBIAS=2.5V; Note 4		0.05		pF
Level Shifting Input Capacitance, Capacitance to GND	CIN, DDC	5V_SUPPLY= 5.0V, Measured at 100KHz, VBIAS=2.5V; Note 2		3.5	4	pF
Level Shifting Input Capacitance, Capacitance to GND	CIN, CEC	5V_SUPPLY=5.0V, Measured at 100KHz, VBIAS=2.5V		3.5	4	pF
Level Shifting Input Capacitance, Capacitance to GND	CIN, HP	5V_SUPPLY=5.0V, Measured at 100KHz, VBIAS=2.5V		3.5	4	pF

Notes: 1. Operating Characteristics are over Standard Operating Conditions unless otherwise specified.
2. Standard IEC 61000-4-2, $C_{DISCHARGE}$=150pF, $R_{DISCHARGE}$=330Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND=0V and ESD_BYP (pin 39), 5V_OUT (pin 0), and HOTPLUG_DET_OUT (pin 22) each bypassed with a 0.1μF ceramic capacitor connected to GND.
3. These measurements performed with no external capacitor on ESD_BYP.
4. Intra-pair matching, each TMDS pair (i.e. D+, D-)

■ TYPICAL APPLICATION CIRCUIT