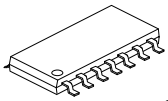
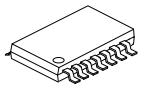
U74CBT3126

CMOS IC

QUADRUPLE FET BUS SWITCH



SOP-14U



TSSOP-14U

■ DESCRIPTION

The **U74CBT3126** is a quadruple line bus switch. It is composed of four 1-bit line switchs with independent separate output-enable (OE) inputs. When OE is low, the switch is disabled.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor and the minimum value of the resistor is determined by the current-sourcing capability of the driver.

■ FEATURES

* 5 Ω switch connection between two ports
* Max t_{pd} of 0.25 ns at 5V
* Low power consumption, I_{CC} = 3 μA (Max.) at 5.5V
* TTL compatible input levels

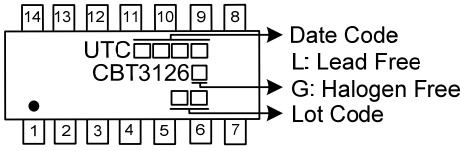
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBT3126L-UEA-R	U74CBT3126G-UEA-R	SOP-14U	Tape Reel
U74CBT3126L-UEB-R	U74CBT3126G-UEB-R	TSSOP-14U	Tape Reel

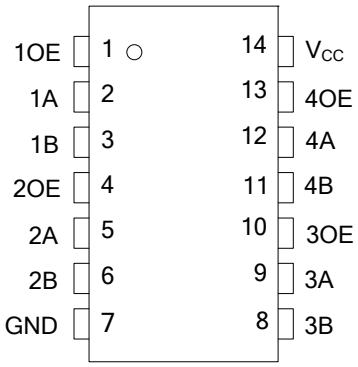
U74CBT3126G-UEA-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) UEA: SOP-14U, UEB: TSSOP-14U
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



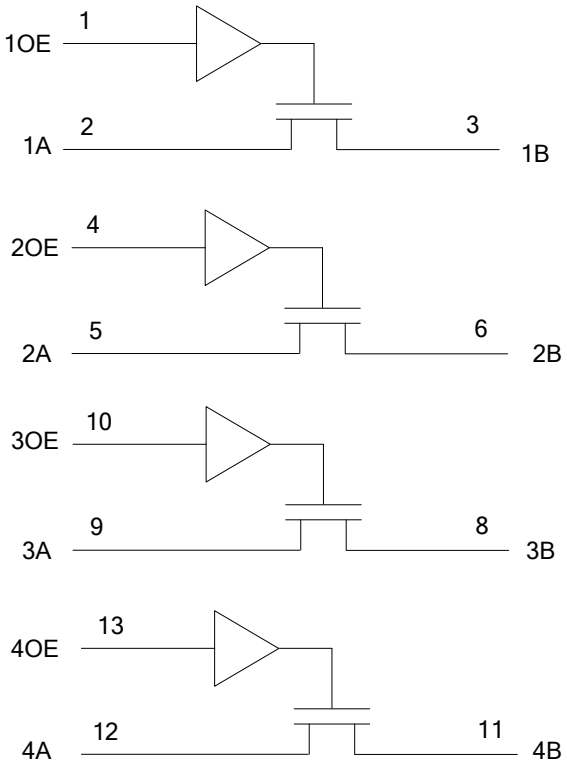
■ PIN CONFIGURATION



■ FUNCTION TABLE (each bus switch)

INPUT OE	FUNCTION
L	Z
H	A=B

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A =25°C , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5 ~ 7	V
Input Voltage		V_{IN}	-0.5 ~ 7	V
Supply Voltage		V_{CC}	4 ~ 5.5	V
Control Input Voltage	High	V_{IH}	2	V
	Low	V_{IL}	0.8	V
Input Clamp Current		I_{IK}	-50	mA
Continuous Channel Current		I_{CH}	128	mA
Operating Temperature		T_{OPR}	-40 ~ +125	°C
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junctions to Ambient	SOP-14U	θ_{JA}	110	°C/W
	TSSOP-14U		135	°C/W

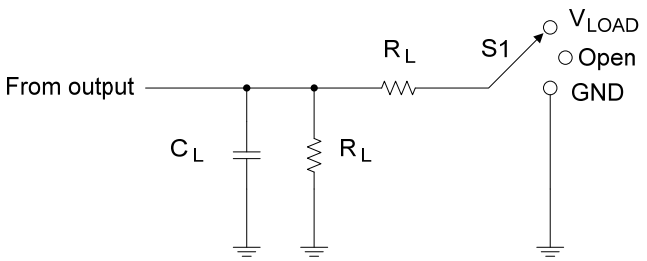
■ ELECTRICAL CHARACTERISTICS (T_A =25°C , V_{CC} = 5 V, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input Diode Voltage	V_{IK}	V_{CC} = 4.5V, I_I = -18mA			-1.2	V
Input Leakage Current (OE inputs)	$I_{I(LEAK)}$	V_{CC} = 5.5V, V_{IN} = 5.5V or GND			±1	μA
Quiescent Supply Current	I_{CC}	V_{CC} = 5.5V, V_{IN} = 5.5V or GND, I_{OUT} = 0			3	μA
Additional quiescent Supply Current	ΔI_{CC}	V_{CC} = 5.5V, One input at 3.4V, Other inputs at V_{CC} or GND			2.5	mA
Input Capacitance (OE)	C_{IN}	V_{IN} = 3V or GND		3		pF
I/O Capacitance (OFF)	C_{IO}	V_{OUT} = 3V or GND, OE = GND		4		pF
Resistor between two ports	r_{on}	V_{CC} = 4V, V_{IN} = 2.4V, I_{IN} = 15mA, TYP at V_{CC} = 4V		16	22	Ω
		V_{CC} = 4.5V, V_{IN} = 0V, I_{IN} = 64mA		5	7	Ω
		V_{CC} = 4.5V, V_{IN} = 0V, I_{IN} = 30mA		5	7	Ω
		V_{CC} = 4.5V, V_{IN} = 2.4V, I_{IN} = 15mA		10	15	Ω

■ SWITCHING CHARACTERISTICS (T_A =25°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
Propagation delay from input A (or B) to output B (or A)	t_{PLH}/t_{PHL} (t_{pd})	C_L=50pF, R_L=500Ω	V_{CC}=4V		0.35	ns
			V_{CC}=5±0.5V		0.25	
Propagation delay from input OE to output A or B	t_{PZL}/t_{PZH} (t_{en})		V_{CC}=4V		5.4	ns
			V_{CC}=5±0.5V	1.6	5.1	
Propagation delay from input OE to output A or B	t_{PLZ}/t_{PHZ} (t_{dis})		V_{CC}=4V		5	ns
			V_{CC}=5±0.5V	1	4.5	

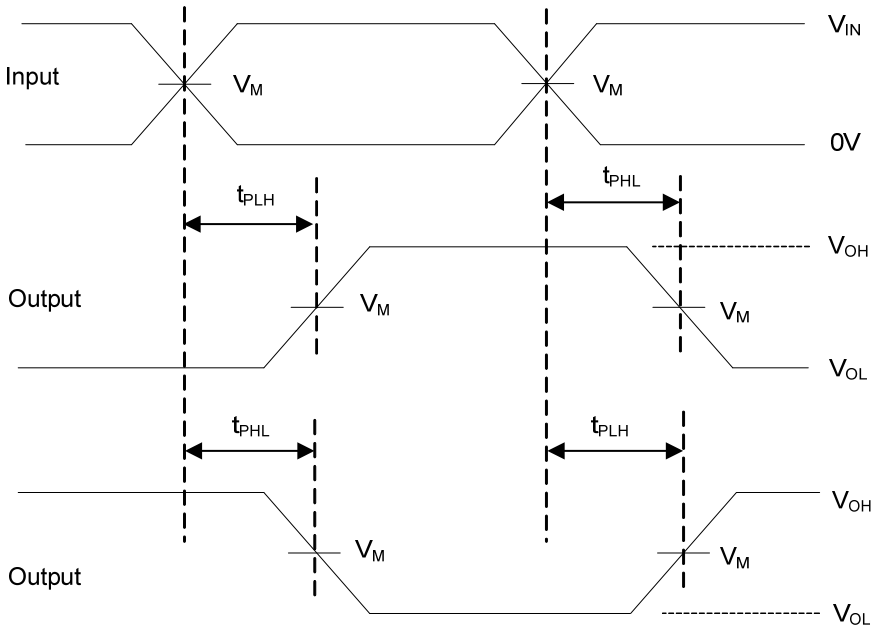
■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

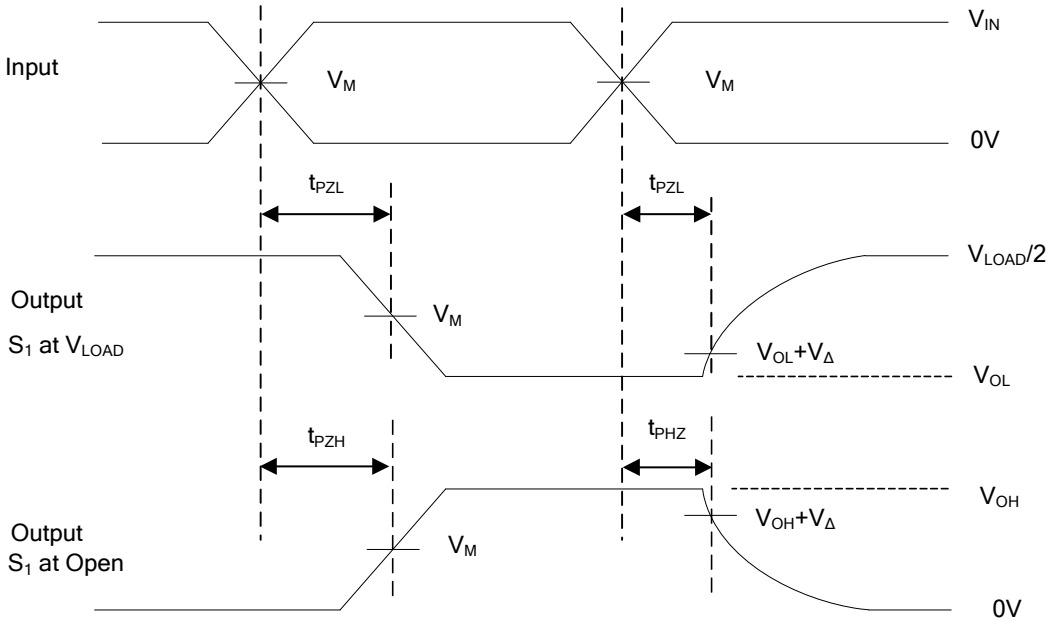
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	Open

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_r, t_f					
4V	V_{CC}	≤2.5ns	1.5V	7V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	1.5V	7V	50pF	500Ω	0.3V



Voltage waveforms Propagation delay times

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.