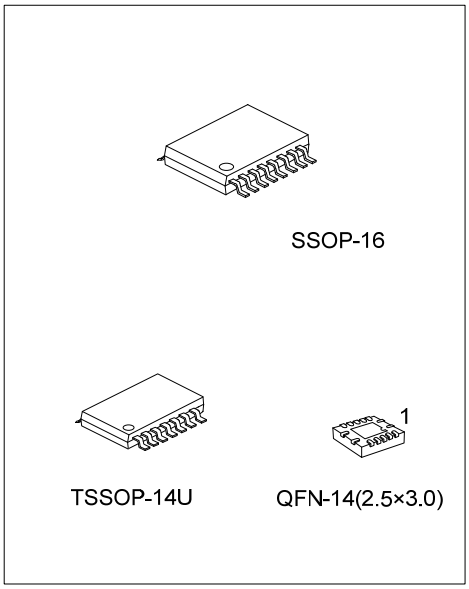
U74CBTLV3126

CMOS IC

LOW-VOLTAGE QUADRUPLE FET BUS SWITCH



■ DESCRIPTION

The **U74CBTLV3126** quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

The device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

* 5-Ω Switch Connection Between Two Ports
* Standard ‘126-Type Pinout
* I_{OFF} Supports Partial-Power-Down Mode Operation

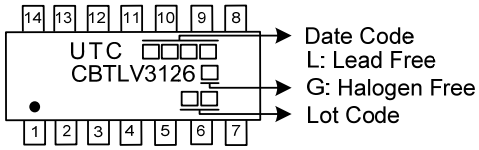
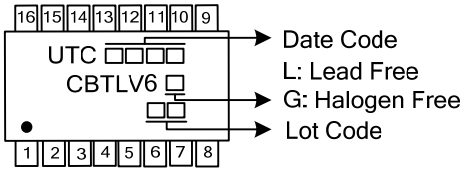
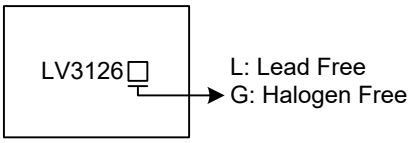
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBTLV3126L-UEB-R	U74CBTLV3126G-UEB-R	TSSOP-14U	Tape Reel
U74CBTLV3126L-R16-R	U74CBTLV3126G-R16-R	SSOP-16	Tape Reel
U74CBTLV3126L-QAF-R	U74CBTLV3126G-QAF-R	QFN-14(2.5×3.0)	Tape Reel

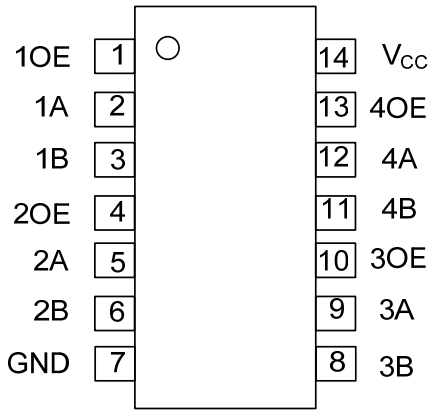
U74CBTLV3126G-UEB-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) UEB: TSSOP-14U, R16: SSOP-16
QAF: QFN-14(2.5×3.0)
(3) G: Halogen Free and Lead Free, L: Lead Free

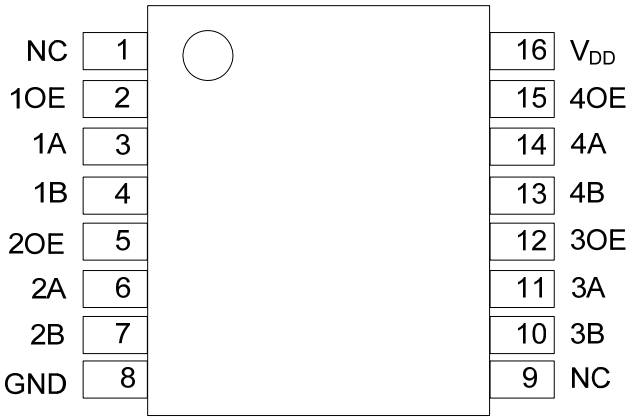
■ MARKING

PACKAGE	MARKING
TSSOP-14U	
SSOP-16	
QFN-14(2.5×3.0)	

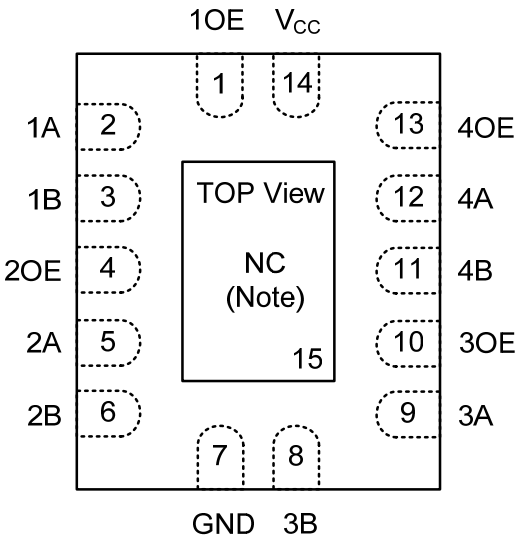
■ PIN CONFIGURATION



TSSOP-14U



SSOP-16

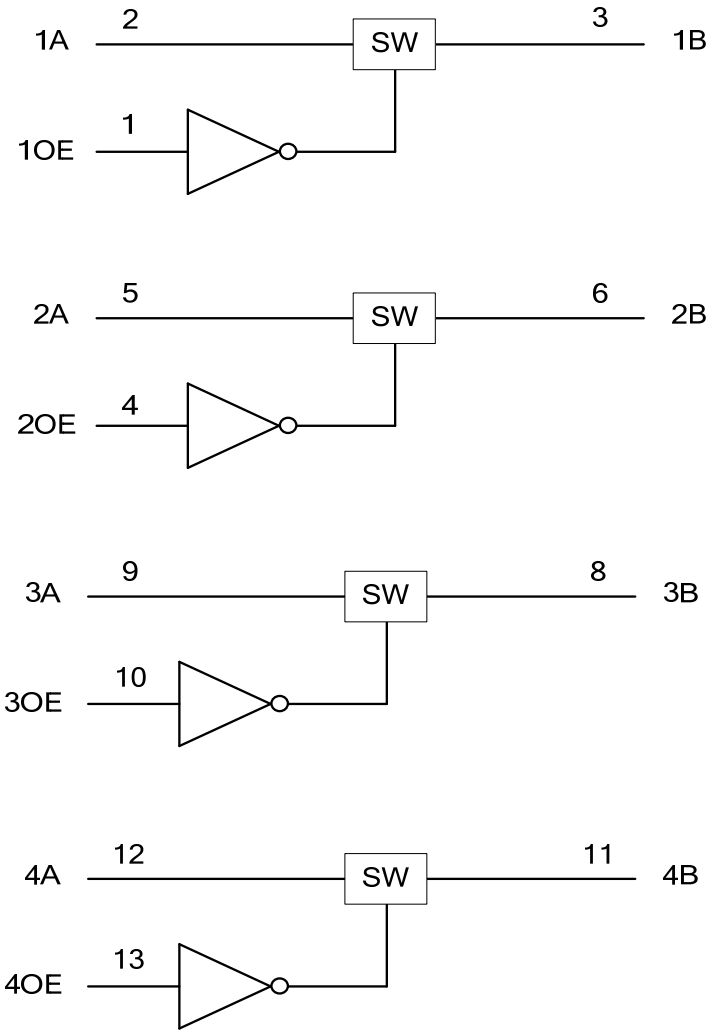


QFN-14(2.5×3.0)

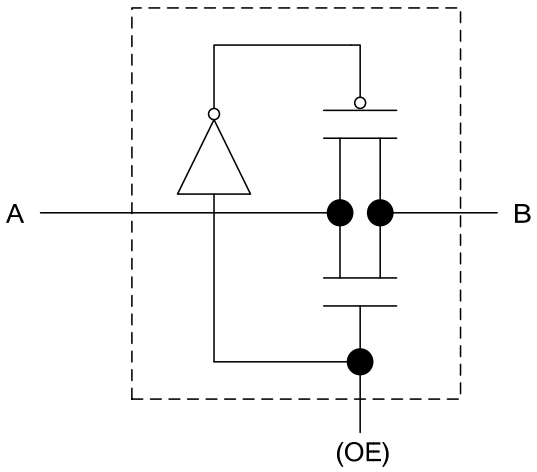
■ FUNCTION TABLE (each bus switch)

INPUT OE	FUNCTION
H	A port = B port
L	Disconnect

■ LOGIC DIAGRAM (positive logic)



■ SIMPLIFIED SCHEMATIC (each FET switch)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 4.6	V
Input Voltage	V_I	-0.5 ~ 4.6	V
Continuous channel current		128	mA
Input Clamp Current($V_{I/O}$<0)	I_{IK}	-50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TSSOP-14U	θ_{JA}	115	°C/W
	SSOP-16		120	°C/W
	QFN-14(2.5×3.0)		104	°C/W

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.3		3.6	V
High-control input voltage	V_{IH}	V_{CC}=2.3V~2.7V	1.7			V
		V_{CC}=2.7V~3.6V	2			V
Low-control input voltage	V_{IL}	V_{CC}=2.3V~2.7V			0.7	V
		V_{CC}=2.7V~3.6V			0.8	V
Operating Temperature	T_A		-40		+125	°C

Note: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ STATIC CHARACTERISTICS

PARAMETER		SYMBOL	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Digital Input Diode Voltage		V_{IK}	V_{CC} =3V, I_I=-18mA					-1.2	V
Input Leakage Current		I_I	V_{CC}=3.6V, V_I=V_{CC} or GND					±1	μA
Power off Leakage Current		I_{OFF}	V_{CC}=0,V_I or V_O=0 to 3.6V					10	μA
Quiescent Supply Current		I_{CC}	V_{CC}=3.6V, V_I= V_{CC} or GND, I_O=0					10	μA
Additional Quiescent Supply Current	Control inputs	ΔI_{CC}	V_{CC}=3.6V, One input at 3V, Other inputs at V_{CC} or GND					300	μA
Control input Capacitance	Control inputs	C_I	V_O=3V or 0				2.5		pF
I/O Capacitance (OFF)		$C_{IO(OFF)}$	V_O=3V or 0, OE=GND				7		pF
Resistor between two ports		R_{ON}	V_{CC}=2.3V Typ. at V_{CC}=2.5V	V_I=0	I_I=64mA		5	8	Ω
					I_I=24mA		5	8	Ω
				V_I=1.7V	I_I=-15mA		27	40	Ω
			V_{CC}=3V	V_I=0V	I_I=64mA		5	7	Ω
					I_I=24mA		5	7	Ω
				V_I=2.4V	I_I=-15mA		10	15	Ω

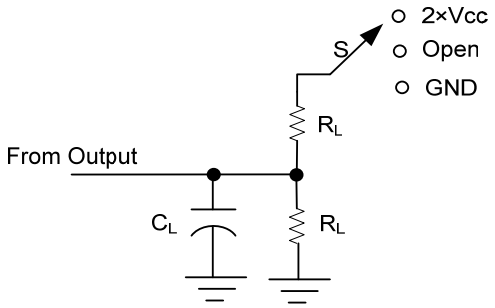
Note: All typical values are at V_{CC}=3.3V, T_A=25°C, unless otherwise specified.

■ DYNAMIC CHARACTERISTICS

See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From input (A or B) to output (B or A)	t_{pd} (t_{PLH}/t_{PHL})	V_{CC}=2.5V±0.2V			0.15	ns
		V_{CC}=3.3V±0.3V			0.25	ns
From input (OE) to output (A or B)	t_{en} (t_{PZL}/t_{PZH})	V_{CC}=2.5V±0.2V	1.6		4.5	ns
		V_{CC}=3.3V±0.3V	1.9		4.2	ns
From input (OE) to output (A or B)	t_{dis} (t_{PLZ}/t_{PHZ})	V_{CC}=2.5V±0.2V	1.3		4.7	ns
		V_{CC}=3.3V±0.3V	1.0		4.8	ns

■ TEST CIRCUIT AND WAVEFORMS

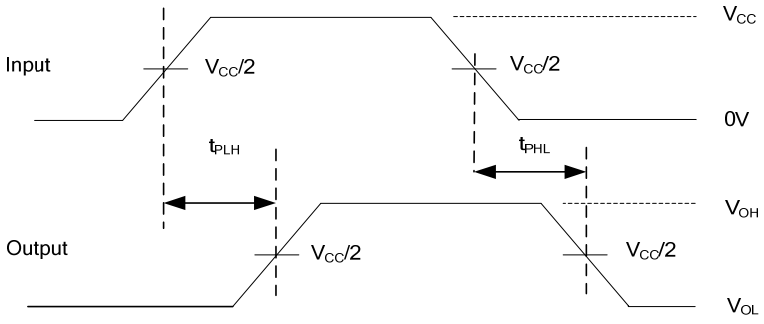


V_{CC}	R_L	C_L	VΔ
2.5V±0.2V	500	30pF	0.15V
3.3V±0.3V	500	50pF	0.3V

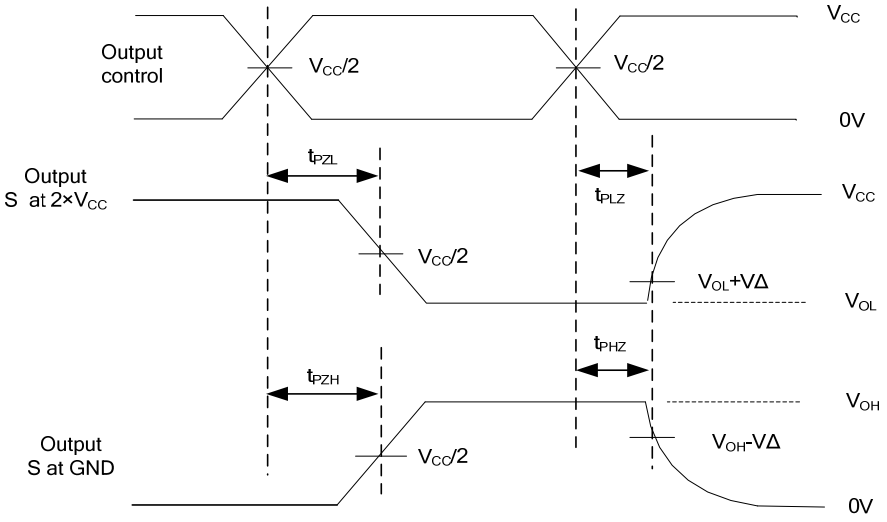
TEST	S
t_{PD}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	2×Vcc

Note: C_L includes probe and jig capacitance.
t_{PLZ} and t_{PHZ} are the same as t_{dis}.
t_{PZL} and t_{PZH} are the same as t_{en}.
t_{PLH} and t_{PHL} are the same as t_{PD}.

Fig. 1 Load circuitry for switching times



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Note: All input pulses are supplied by generators having the following characteristics:
t_r, t_f ≤ 2ns; P_{RR} ≤ 10MHz; Z_O = 50Ω.

Fig. 2 Propagation delay from input(A) to output(B) and Output transition time