



U74HC164

CMOS IC

8-BIT SERIAL-IN AND PARALLEL-OUT SHIFT REGISTER

DESCRIPTION

The **U74HC164** is an 8-bit serial-in/parallel-out shift register. The logical AND of the DSA and DSB enters into Q0 and shifts one

place to right on each LOW-to-HIGH transition of the clock ($\overline{CP}$). A low level on the master reset ($\overline{MR}$) input clears all the registers asynchronously and force all outputs LOW.

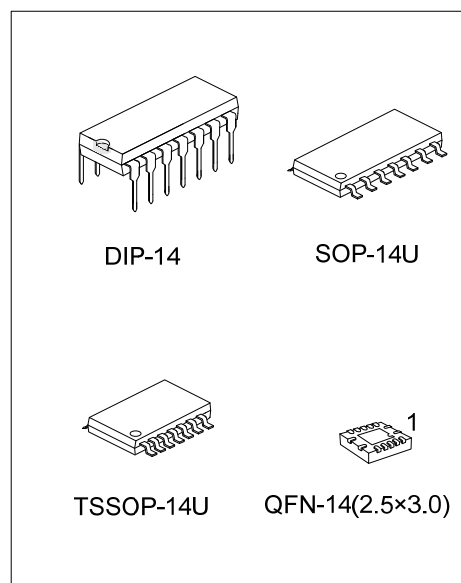
FEATURES

- * Operation Voltage Range: 2 ~ 6V
- * Asynchronous Reset Input

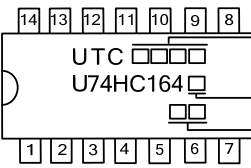
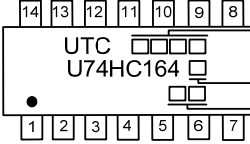
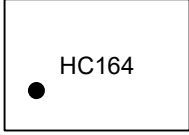
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC164L-D14-T	U74HC164G-D14-T	DIP-14	Tube
U74HC164L-UEA-R	U74HC164G-UEA-R	SOP-14U	Tape Reel
U74HC164L-UEB-R	U74HC164G-UEB-R	TSSOP-14U	Tape Reel
U74HC164L-QAF-R	U74HC164G-QAF-R	QFN-14(2.5×3.0)	Tape Reel

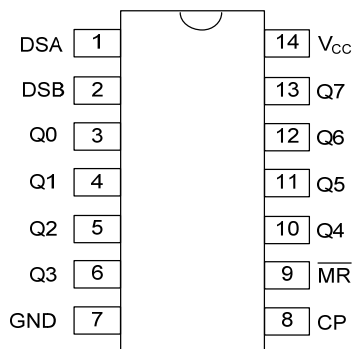
U74HC164G-D14-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube, R: Tape Reel (2) DIP: DIP-14, UEA: SOP-14U, UEB: TSSOP-14U QAF: QFN-14(2.5×3.0) (3) G: Halogen Free and Lead Free, L: Lead Free
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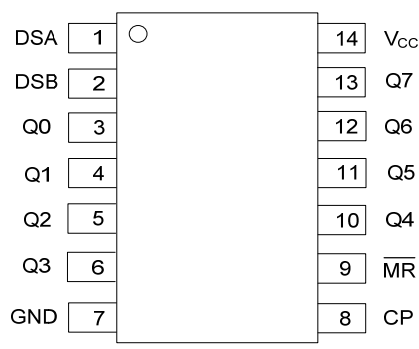
MARKING

PACKAGE	MARKING
DIP-14	 → Date Code L: Lead Free G: Halogen Free → Lot Code
SOP-14U TSSOP-14U	 → Date Code L: Lead Free G: Halogen Free → Lot Code
QFN-14(2.5×3.0)	 HC164

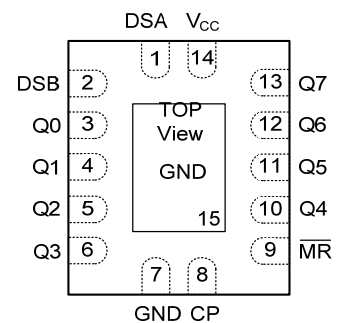
PIN CONFIGURATION



DIP-14



SOP-14U / TSSOP-14U



QFN-14(2.5×3.0)

■ FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
RESET (CLEAR)	$\overline{\text{MR}}$	CP	DSA	DSB	Q_0	$Q_1 - Q_7$
Shift	L	X	X	X	L	L - L
	H	↑	l	l	L	$q_0 - q_6$
	H	↑	l	h	L	$q_0 - q_6$
	H	↑	h	l	L	$q_0 - q_6$
	H	↑	h	h	H	$q_0 - q_6$

Notes: H = High voltage level.

L = Low voltage level.

h = High voltage level one set-up time prior to the low-to-high clock transition.

l = Low voltage level one set-up time prior to the low-to-high clock transition.

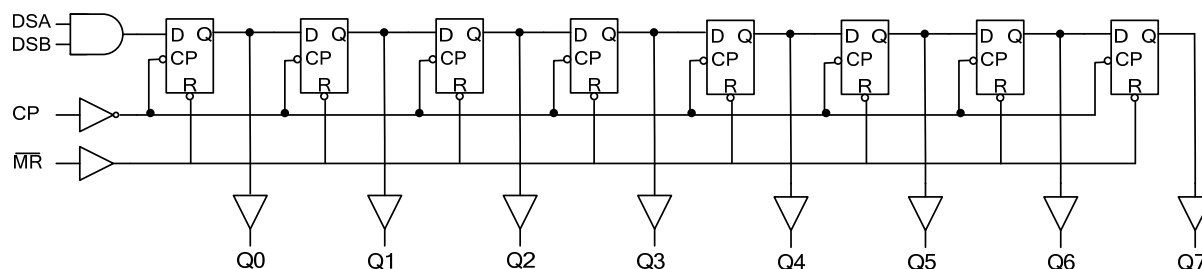
X = Don't care.

↑ = Transition from low to high level.

q_n = Lower case letters indicate the state of the referenced input one set-up time prior to the low-to-high clock transition.

■ FUNCTIONAL DIAGRAM

Logic Diagram



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
V_{CC} or GND Current	I_{CC}	± 50	mA
Output Current	I_{OUT}	± 25	mA
Input Clamp Current	I_{IK}	± 20	mA
Output Clamp Current	I_{OK}	± 20	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0	5.0	6.0	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Time	$\Delta t/\Delta v$	$V_{CC}=2V$			1000	ns
		$V_{CC}=4.5V$			500	ns
		$V_{CC}=6V$			400	ns
Operating Temperature	T_A		-40		+125	°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-14	θ_{JA}	100	°C/W
	SOP-14U		125	°C/W
	TSSOP-14U		150	°C/W
	QFN-14(2.5×3.0)		130	°C/W

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage High-Level	V_{IH}	$V_{CC}=2.0V$	1.5			V
		$V_{CC}=4.5V$	3.15			V
		$V_{CC}=6.0V$	4.2			V
Input Voltage Low-Level	V_{IL}	$V_{CC}=2.0V$			0.5	V
		$V_{CC}=4.5V$			1.35	V
		$V_{CC}=6.0V$			1.8	V
Output Voltage High-Level	V_{OH}	$V_{CC}=2.0V, I_{OH}=-20\mu A$	1.9			V
		$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4			V
		$V_{CC}=6.0V, I_{OH}=-20\mu A$	5.9			V
		$V_{CC}=4.5V, I_{OH}=-4mA$	3.98			V
		$V_{CC}=6.0V, I_{OH}=-5.2mA$	5.48			V
Output Voltage Low-Level	V_{OL}	$V_{CC}=2.0V, I_{OL}=20\mu A$			0.1	V
		$V_{CC}=4.5V, I_{OL}=20\mu A$			0.1	V
		$V_{CC}=6.0V, I_{OL}=20\mu A$			0.1	V
		$V_{CC}=4.5V, I_{OL}=4mA$			0.26	V
		$V_{CC}=6.0V, I_{OL}=5.2mA$			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN}=V_{CC}$ or GND, $V_{CC}=6.0V$			± 0.1	μA
Quiescent Supply Current	I_Q	$V_{IN}=V_{CC}$ or GND, $V_{CC}=6.0V, I_{OUT}=0$			8	μA
Input Capacitance	C_{IN}				10	pF

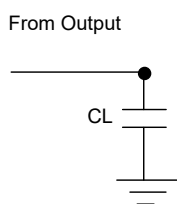
■ DYNAMIC CHARACTERISTICS (GND=0V; $t_R=t_F=6\text{ns}$; $C_L=50\text{pF}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From CP to Qn	t_{PHL}, t_{PLH}	$V_{CC}=2.0\text{V}$		41	170	ns
		$V_{CC}=4.5\text{V}$		15	34	ns
		$V_{CC}=6.0\text{V}$		12	29	ns
Propagation Delay From $\overline{\text{MR}}$ to Qn	t_{PHL}	$V_{CC}=2.0\text{V}$		39	140	ns
		$V_{CC}=4.5\text{V}$		14	28	ns
		$V_{CC}=6.0\text{V}$		11	24	ns
Output Transition Time	t_{THL}, t_{TLH}	$V_{CC}=2.0\text{V}$		19	75	ns
		$V_{CC}=4.5\text{V}$		7	15	ns
		$V_{CC}=6.0\text{V}$		6	13	ns
Clock Pulse Width High or Low	t_W	$V_{CC}=2.0\text{V}$	80	14		ns
		$V_{CC}=4.5\text{V}$	16	5		ns
		$V_{CC}=6.0\text{V}$	14	4		ns
Master Reset Pulse Width Low	t_W	$V_{CC}=2.0\text{V}$	60	17		ns
		$V_{CC}=4.5\text{V}$	12	6		ns
		$V_{CC}=6.0\text{V}$	10	5		ns
Removal Time $\overline{\text{MR}}$ to CP	t_{rem}	$V_{CC}=2.0\text{V}$	60	17		ns
		$V_{CC}=4.5\text{V}$	12	6		ns
		$V_{CC}=6.0\text{V}$	10	5		ns
Setup Time DSA and DSB to CP	t_{SU}	$V_{CC}=2.0\text{V}$	60	8		ns
		$V_{CC}=4.5\text{V}$	12	3		ns
		$V_{CC}=6.0\text{V}$	10	2		ns
Hold Time DSA and DSB to CP	t_{H}	$V_{CC}=2.0\text{V}$	+4	-6		ns
		$V_{CC}=4.5\text{V}$	+4	-2		ns
		$V_{CC}=6.0\text{V}$	+4	-2		ns
Maximum Clock Pulse Frequency	f_{MAX}	$V_{CC}=2.0\text{V}$	6	23		MHz
		$V_{CC}=4.5\text{V}$	30	71		MHz
		$V_{CC}=6.0\text{V}$	35	85		MHz
Clock Frequency	f_{CLOCK}	$V_{CC}=2.0\text{V}$			6	MHz
		$V_{CC}=4.5\text{V}$			31	MHz
		$V_{CC}=6.0\text{V}$			36	MHz

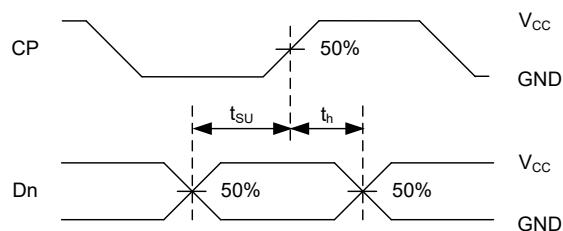
■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load		40		pF

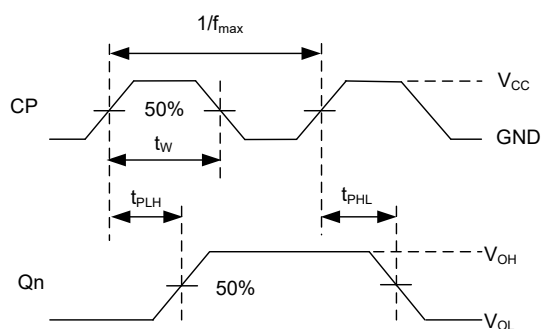
■ TEST CIRCUIT AND WAVEFORMS



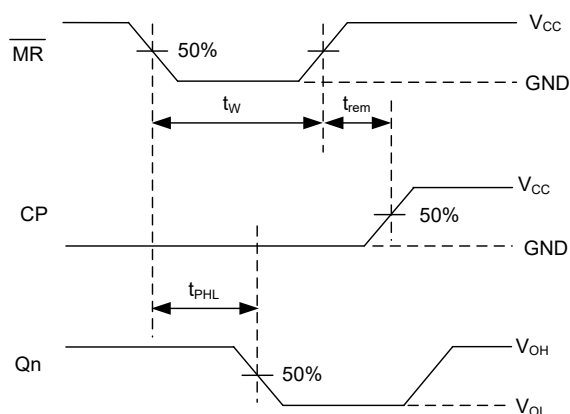
TEST CIRCUIT



SETUP TIME AND HOLD TIME



PROPAGATION DELAY TIMES FROM CP TO Qn



PROPAGATION DELAY TIMES FROM $\overline{MR}$ TO Qn

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