

**U74LVC07A****CMOS IC****HEX BUFFERS WITH
OPEN-DRAIN OUTPUTS****■ DESCRIPTION**

The **U74LVC07A** contain six independent buffers with open drain outputs. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions

Inputs can be driven from 1.8V, 2.5V, 3.3V, or 5V devices. This feature allows the use of these devices as translators in a mixed-system environment.

■ FEATURES

- * Operate from 1.65V to 5.5V
- * Inputs and open-drain outputs accept voltages to 5.5V
- * Direct interface with TTL levels
- * I_{off} supports partial-power-down mode

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC07AL-UEA-R	U74LVC07AG-UEA-R	SOP-14U	Tape Reel
U74LVC07AL-UEB-R	U74LVC07AG-UEB-R	TSSOP-14U	Tape Reel

U74LVC07AG-UEA-R

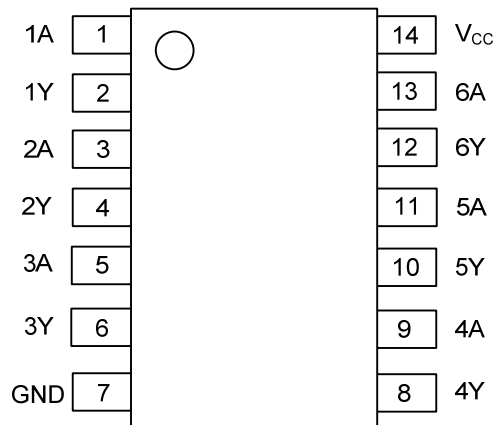
- (1) Packing Type
- (2) Package Type
- (3) Green Package

- (1) R: Tape Reel
- (2) UEA: SOP-14U, UEB: TSSOP-14U
- (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

SOP-14U	TSSOP-14U
14 13 12 11 10 9 8 UTC □ □ □ □ U74LVC07A □ ● □ □ □ 1 2 3 4 5 6 7 → Date Code → L: Lead Free → G: Halogen Free → Lot Code	14 13 12 11 10 9 8 UTC □ □ □ □ U74LVC07A □ ● □ □ □ 1 2 3 4 5 6 7 → Date Code → L: Lead Free → G: Halogen Free → Lot Code

■ PIN CONFIGURATION

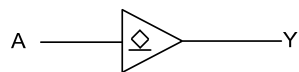


■ FUNCTION TABLE (each buffer)

INPUT(A)	OUTPUT(Y)
H	Z
L	L

Note: H: HIGH voltage level; L: LOW voltage level; Z=high-impedance OFF-state.

■ LOGIC DIAGRAM (each inverter)



Logic symbol

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5 ~ +6.5	V
Input Voltage	V _{IN}	-0.5 ~ +6.5	V
Output Voltage	V _{OUT}	-0.5 ~ +6.5	V
V _{CC} or GND Current	I _{CC}	±100	mA
Continuous Output Current (V _{OUT} =0 to V _{CC})	I _{OUT}	±50	mA
Input Clamp Current (V _{IN} <0)	I _{IK}	-50	mA
Output Clamp Current (V _{OUT} <0)	I _{OK}	-50	mA
Storage Temperature Range	T _{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}	Operating	1.65		5.5	V
Input Voltage	V _{IN}		0		5.5	V
Output Voltage	V _{OUT}		0		5.5	V
Low-level Output Current	I _{OL}	V _{CC} =1.65V			4	mA
		V _{CC} =2.3V			12	mA
		V _{CC} =2.7V			12	mA
		V _{CC} =3V			24	mA
		V _{CC} =4.5V			24	mA
Input Transition Rise or Fall Rate	Δt/Δv	V _{CC} =1.65V~2.7V			20	ns/V
		V _{CC} =2.7V~3.6V			10	ns/V
Operating Temperature	T _A		-40		+125	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-14U	125	°C/W
	TSSOP-14U	150	°C/W

■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	$V_{CC}=1.65\text{V} \sim 1.95\text{V}$	$0.65 \times V_{CC}$			V
		$V_{CC}=2.3\text{V} \sim 2.7\text{V}$	1.7			V
		$V_{CC}=2.7\text{V} \sim 3.6\text{V}$	2			V
		$V_{CC}=4.5\text{V} \sim 5.5\text{V}$	$0.7 \times V_{CC}$			V
Low-level Input Voltage	V_{IL}	$V_{CC}=1.65\text{V} \sim 1.95\text{V}$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.3\text{V} \sim 2.7\text{V}$			0.7	V
		$V_{CC}=2.7\text{V} \sim 3.6\text{V}$			0.8	V
		$V_{CC}=4.5\text{V} \sim 5.5\text{V}$			$0.3 \times V_{CC}$	V
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65 \sim 5.5\text{V}$, $I_{OL}=100\mu\text{A}$			0.2	V
		$V_{CC}=1.65\text{V}$, $I_{OL}=4\text{mA}$			0.45	V
		$V_{CC}=2.3\text{V}$, $I_{OL}=12\text{mA}$			0.7	V
		$V_{CC}=2.7\text{V}$, $I_{OL}=12\text{mA}$			0.4	V
		$V_{CC}=3.0\text{V}$, $I_{OL}=24\text{mA}$			0.55	V
		$V_{CC}=4.5\text{V}$, $I_{OL}=32\text{mA}$			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN}=5.5\text{V}$ or GND, $V_{CC}=3.6\text{V}$			± 5	μA
Power OFF Leakage Current	I_{OFF}	V_{IN} or $V_{OUT}=5.5\text{V}$, $V_{CC}=0\text{V}$			± 10	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$ $V_{CC}=3.6\text{V}$			10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=2.7 \sim 3.6\text{V}$, $I_{OUT}=0$ One input at $V_{CC}-0.6\text{V}$, Other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_I	$V_{IN}=V_{CC}$ or GND, $V_{CC}=3.3\text{V}$		5		pF

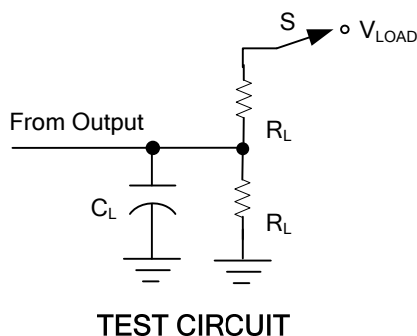
■ **SWITCHING CHARACTERISTICS** ($T_A=-40 \sim +125^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay from Input (nA) to Output (nY)	t_{PLZ} / t_{PZL}	$V_{CC}=1.8 \pm 0.15\text{V}$, $C_L=30\text{pF}$, $R_L=1\text{K}\Omega$	1		8.0	ns
		$V_{CC}=2.5 \pm 0.2\text{V}$, $C_L=30\text{pF}$, $R_L=500\Omega$	1		6.2	ns
		$V_{CC}=2.7\text{V}$, $C_L=50\text{pF}$, $R_L=500\Omega$	1		5.8	ns
		$V_{CC}=3.3 \pm 0.3\text{V}$, $C_L=50\text{pF}$, $R_L=500\Omega$	1		5.6	ns
		$V_{CC}=5 \pm 0.5\text{V}$, $C_L=50\text{pF}$, $R_L=500\Omega$	1		4.6	ns

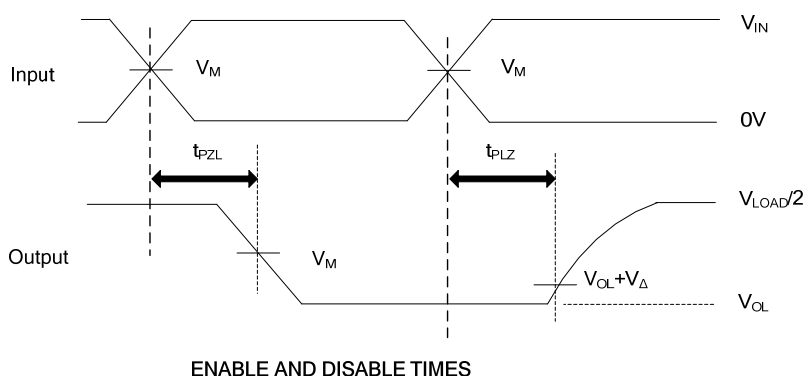
■ **OPERATING CHARACTERISTICS** ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance Per Inverter	C_{PD}	$V_{CC}=1.8 \pm 0.15\text{V}$, $f=10\text{MHz}$		1.8		pF
		$V_{CC}=2.5 \pm 0.2\text{V}$, $f=10\text{MHz}$		2.0		pF
		$V_{CC}=3.3 \pm 0.3\text{V}$, $f=10\text{MHz}$		2.5		pF

■ TEST CIRCUIT AND WAVEFORMS



V_{CC}	Inputs		V_M	V_{LOAD}	V_{Δ}	C_L	R_L
	V_{IN}	t_R, t_F					
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	$0.15V$	$30pF$	$1K\Omega$
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	$0.15V$	$30pF$	500Ω
$2.7V$	$2.7V$	$\leq 2.5ns$	$1.5V$	$2 \times V_{CC}$	$0.3V$	$50pF$	500Ω
$3.3V \pm 0.3V$	$2.7V$	$\leq 2.5ns$	$1.5V$	$2 \times V_{CC}$	$0.3V$	$50pF$	500Ω
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	$0.3V$	$50pF$	500Ω



Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10MHz$, $Z_0 = 50\Omega$.

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