

**U74LVC126A****CMOS IC****QUADRUPLE BUS BUFFER
GATES WITH 3-STATE
OUTPUTS****DESCRIPTION**

The **U74LVC126A** are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. When OE is low, the nY outputs are in a high-impedance state. When OE is high, the device passes non-inverted data from the nA input to its nY output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3V to 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

FEATURES

- * 1.65V to 3.6V V_{CC} Operation
- * Max t_{PD} of 4.7ns from A to Y at $V_{CC} = 3.3V$, $C_L = 50pF$, $R_L = 500\Omega$
- * $\pm 24mA$ output driver at 3V

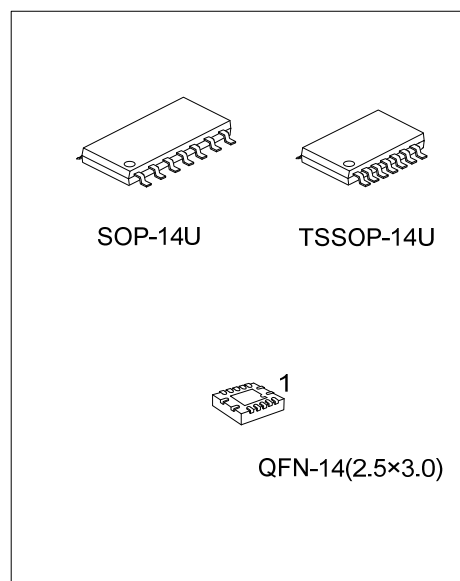
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC126AL-UEA-R	U74LVC126AG-UEA-R	SOP-14U	Tape Reel
U74LVC126AL-UEB-R	U74LVC126AG-UEB-R	TSSOP-14U	Tape Reel
U74LVC126AL-QAF-R	U74LVC126AG-QAF-R	QFN-14(2.5×3.0)	Tape Reel

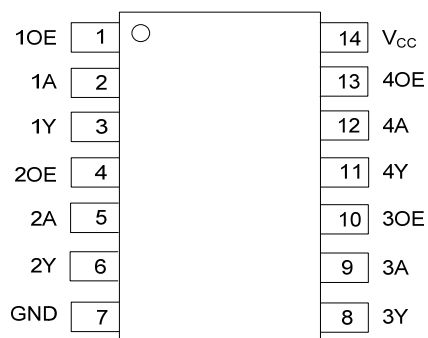
U74LVC126AG-UEA-R (1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) UEA: SOP-14U, UEB: TSSOP-14U QAF: QFN-14(2.5×3.0) (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

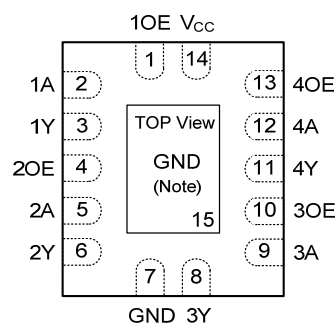
SOP-14U / TSSOP-14U	QFN-14(2.5×3.0)
14 13 12 11 10 9 8 UTC □ □ □ □ → Date Code LVC126A □ → L: Lead Free □ □ → G: Halogen Free □ □ → Lot Code 1 2 3 4 5 6 7	LVC126A



PIN CONFIGURATION



SOP-14U / TSSOP-14U



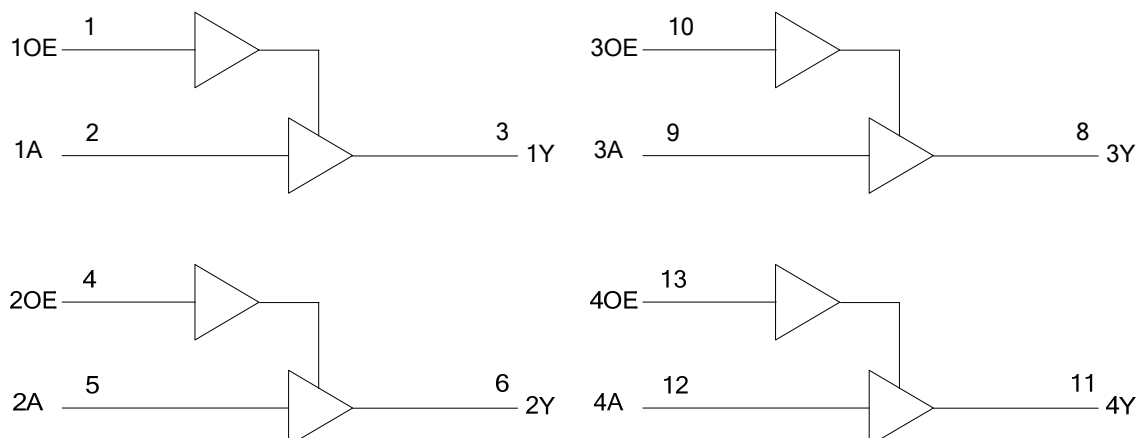
QFN-14(2.5x3.0)

Note: Connect exposed pad to GND

FUNCTION TABLE

INPUT		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~6.5	V
Input Voltage	V_{IN}	-0.5~6.5	V
Output Voltage	V_{OUT}	-0.5~ V_{CC} +0.5	V
Input Clamp Current ($V_{IN}<0$)	I_{IK}	-50	mA
Output Clamp Current ($V_{OUT}<0$, or $V_{OUT}>V_{CC}$)	I_{OK}	-50	mA
Output Current	I_{OUT}	± 50	mA
V_{CC} or GND Current	I_{CC}	± 100	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junctions to Ambient	SOP-14U	100	°C/W
	TSSOP-14U	130	°C/W
	QFN-14(2.5×3.0)	104	°C/W

■ RECOMMENDED OPERATING COMDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		3.6	V
		Data retention only	1.5			
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
High-Level Output Current	I_{OH}	$V_{CC}=1.65V$			-4	mA
		$V_{CC}=2.3V$			-8	mA
		$V_{CC}=2.7V$			-12	mA
		$V_{CC}=3V$			-24	mA
Low-Level Output Current	I_{OL}	$V_{CC}=1.65V$			4	mA
		$V_{CC}=2.3V$			8	mA
		$V_{CC}=2.7V$			12	mA
		$V_{CC}=3V$			24	mA
Input Transition Rise or Fall Rate	$\Delta t/\Delta V$		0		10	ns/V
Operating Temperature	T_A		-40		+125	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Input Voltage	V _{IH}	V _{CC} =1.65V ~ 1.95V	V _{CC} ×0.65			V _{CC} ×0.65			V
		V _{CC} =2.3V ~ 2.7V	1.7			1.7			V
		V _{CC} =2.7V ~ 3.6V	2			2			V
Low-Level Input Voltage	V _{IL}	V _{CC} =1.65V ~ 1.95V			V _{CC} ×0.35			V _{CC} ×0.35	V
		V _{CC} =2.3V ~ 2.7V			0.7			0.7	V
		V _{CC} =2.7V ~ 3.6V			0.8			0.8	V
High-Level Output Voltage	V _{OH}	V _{CC} =1.65V ~ 3.6V, I _{OH} =-100μA	V _{CC} -0.2			V _{CC} -0.3			V
		V _{CC} =1.65V, I _{OH} =-4mA	1.2			1.05			V
		V _{CC} =2.3V, I _{OH} =-8mA	1.7			1.55			V
		V _{CC} =2.7V, I _{OH} =-12mA	2.2			2.05			V
		V _{CC} =3V, I _{OH} =-12mA	2.4			2.25			V
		V _{CC} =3V, I _{OH} =-24mA	2.3			2			V
Low-Level Output Voltage	V _{OL}	V _{CC} =1.65V ~ 3.6V, I _{OL} =100μA			0.1			0.3	V
		V _{CC} =1.65V, I _{OL} =4mA			0.45			0.6	V
		V _{CC} =2.3V, I _{OL} =8mA			0.7			0.8	V
		V _{CC} =2.7V, I _{OL} =12mA			0.4			0.6	V
		V _{CC} =3V, I _{OL} =24mA			0.55			0.8	V
Input Leakage Current (A or OE input)	I _{I(LEAK)}	V _{IN} =5.5V or GND, V _{CC} =3.6V			±1			±20	μA
High-impedance state Current	I _{OZ}	V _{OUT} =V _{CC} or GND, V _{CC} =3.6V			±1			±20	μA
Quiescent Supply Current	I _{CC}	V _{IN} =V _{CC} or GND, I _{OUT} =0, V _{CC} =3.6V			1			40	μA
Additional quiescent supply current	ΔI _{CC}	One input at V _{CC} - 0.6V, V _{CC} =2.7V to 3.6V, other inputs at V _{CC} or GND			500			5000	μA

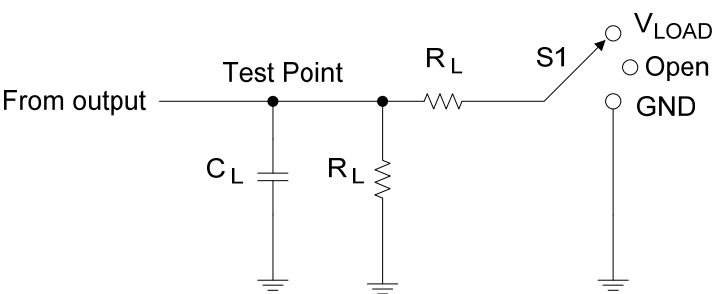
SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay from input A to output Y	t _{PD}	V _{CC} =1.8V			18			20	ns
		V _{CC} =2.5V±0.2V	1		8.2			10.7	ns
		V _{CC} =2.7V	1		6.2			7.7	ns
		V _{CC} =3.3V±0.3V	1		5.7			7.2	ns
Propagation delay from input OE to output Y	t _{EN}	V _{CC} =1.8V			22			24	ns
		V _{CC} =2.5V±0.2V	1		8.3			10.4	ns
		V _{CC} =2.7V	1		6.3			8.3	ns
		V _{CC} =3.3V±0.3V	1		5.7			7.7	ns
Propagation delay from input OE to output Y	t _{DIS}	V _{CC} =1.8V			15			17	ns
		V _{CC} =2.5V±0.2V	1		8.7			10.8	ns
		V _{CC} =2.7V	1		6.7			8.7	ns
		V _{CC} =3.3V±0.3V	1.3		6			7.8	ns
Skew between any two outputs of the same package switching in the same direction	t _{SK(O)}	V _{CC} =3.3V±0.3V			1			1.5	ns

■ **OPERATING CHARACTERISTICS** (f=10MHz, Outputs enable, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C _{IN}	V _{IN} =V _{CC} or GND, V _{CC} =3.3V		4.5		pF
Output Capacitance	C _{OUT}	V _{OUT} =V _{CC} or GND, V _{CC} =3.3V		7		pF
Power dissipation capacitance per gate	C _{PD}	V _{CC} =1.8V		20		pF
		V _{CC} =2.5V		21		pF
		V _{CC} =3.3V		22		pF
		V _{CC} =1.8V		2		pF
		V _{CC} =2.5V		3		pF
		V _{CC} =3.3V		4		pF

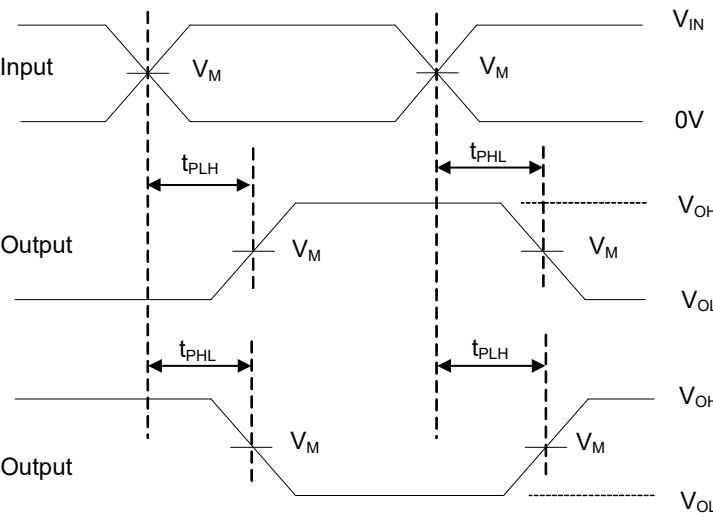
■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

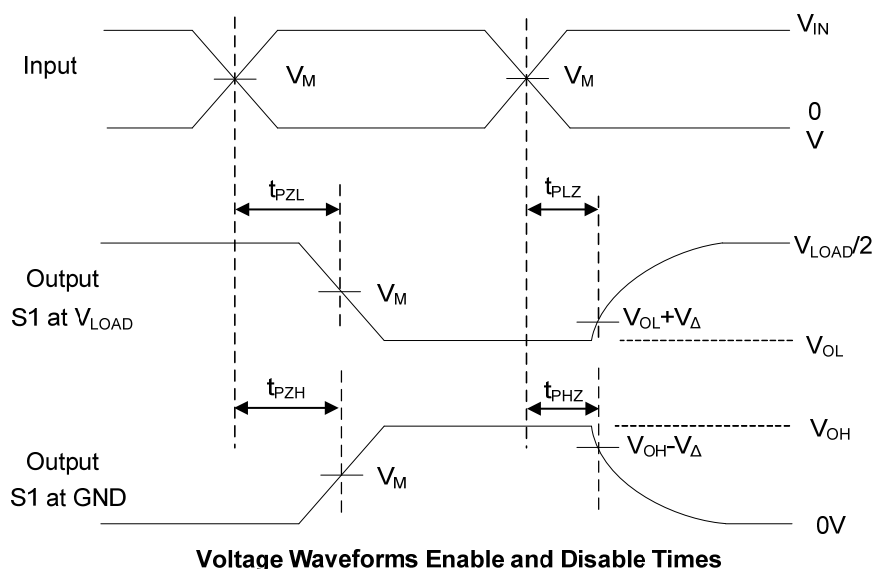
TEST	S1		
	VCC = 1.8V±0.15V	VCC = 2.5V±0.2V	VCC = 2.7V AND 3.3V±0.3V
tPLH/tPHL	Open	Open	Open
tPLZ/tPZL	VLOAD	VLOAD	6V
tPHZ/tPZH	GND	GND	GND

VCC	Input		VM	VLOAD	CL	RL	VΔ
	VIN	tR, tF					
1.8V±0.15V	VCC	≤2ns	VCC/2	2*VCC	30pF	1kΩ	0.15V
2.5V±0.2V	VCC	≤2ns	VCC/2	2*VCC	30pF	500Ω	0.15V
2.7V	VCC	≤2ns	1.5V	6V	50pF	500Ω	0.3V
3.3V±0.3V	VCC	≤2ns	1.5V	6V	50pF	500Ω	0.3V



Voltage Waveforms Propagation Delay Times

■ TEST CIRCUIT AND WAVEFORMS(Cont.)



Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_o = 50\Omega$.

3. t_{PLH} and t_{PHL} are the same as t_{PD} .

4. t_{PZL} and t_{PZH} are the same as t_{EN} .

5. t_{PLZ} and t_{PHZ} are the same as t_{DIS} .

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