

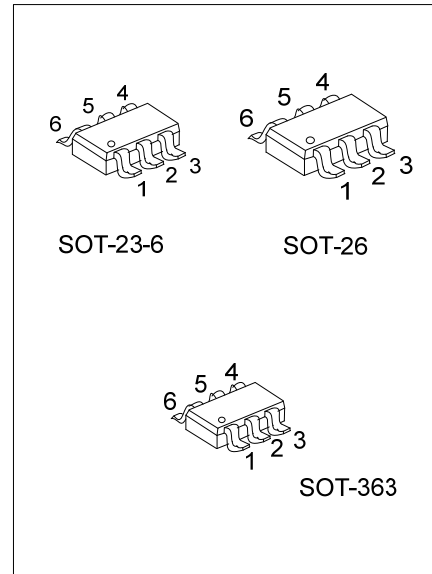
**U74LVC1G57****CMOS IC****MULTIPLE-FUNCTION GATE****DESCRIPTION**

The **U74LVC1G57** provides configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

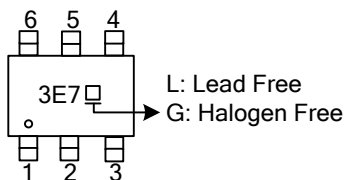
FEATURES

- * Wide supply voltage range from 1.65V to 5.5V
- * Inputs accept voltages up to 5.5V
- * I_{OFF} supports partial-power-down mode
- * Low static power consumption; $I_{CC}=10\mu A$ (Max.)

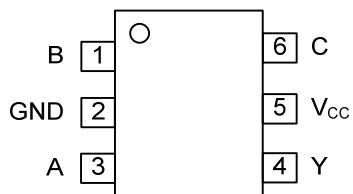
**ORDERING INFORMATION**

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC1G57L-AE6-R	U74LVC1G57G-AE6-R	SOT-23-6	Tape Reel
U74LVC1G57L-AG6-R	U74LVC1G57G-AG6-R	SOT-26	Tape Reel
U74LVC1G57L-AL6-R	U74LVC1G57G-AL6-R	SOT-363	Tape Reel

U74LVC1G57G-AE6-R (1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) AE6: SOT-26, AG6: SOT-26, AL6: SOT-363 (3) G: Halogen Free and Lead Free, L: Lead Free
---	--

MARKING

PIN CONFIGURATION



PIN DESCRIPTION

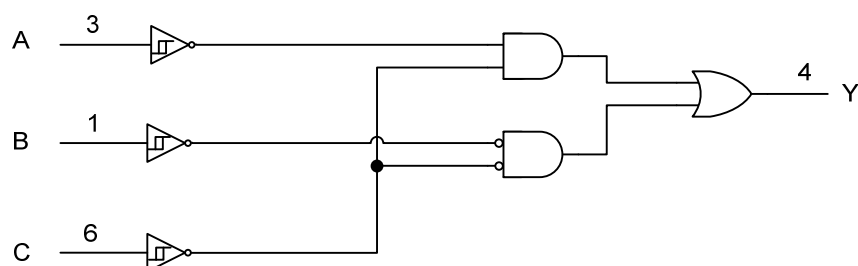
PIN NO.	PIN NAME	I/O	DESCRIPTION
1	B	I	Logic Input 1
2	GND	-	Ground
3	A	I	Logic Input 0
4	Y	O	Logic output
5	V _{CC}	-	Power
6	C	I	Logic Input 2

FUNCTION TABLE

INPUT			OUTPUT
C	B	A	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

Note: H: High voltage level; L: Low voltage level.

LOGIC DIAGRAM (positive logic)



FUNCTION SELECTION TABLE

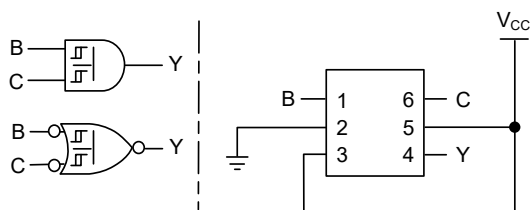


Figure 1. 2-Input AND Gate or 2-Input NOR Gate With Both Inputs Inverted

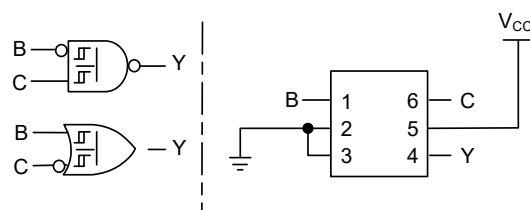


Figure 2. 2-Input NAND Gate With Inverted B Input or 2-Input OR Gate With Inverted C Input

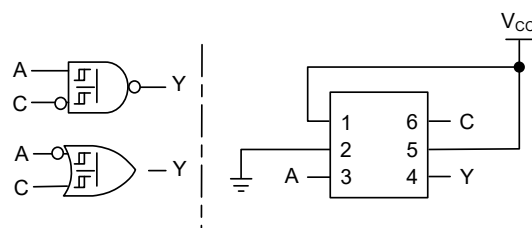


Figure 3. 2-Input NAND Gate With Inverted C Input or 2-Input OR Gate With Inverted A Input

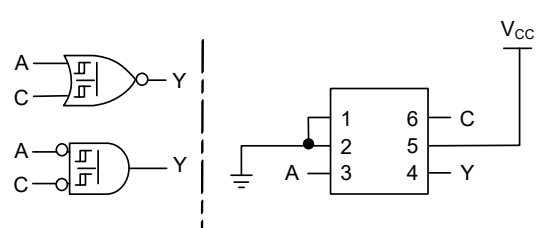


Figure 4. 2-Input NOR Gate or 2-Input AND Gate With Both Inputs Inverted

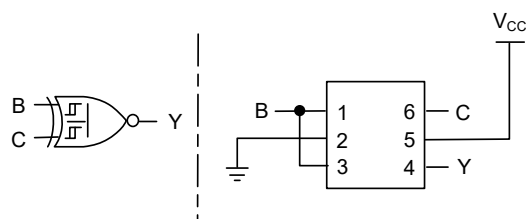


Figure 5. 2-Input XNOR Gate

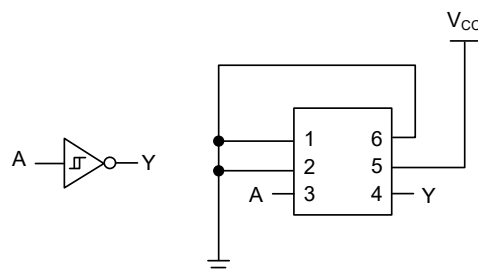


Figure 6. Inverter

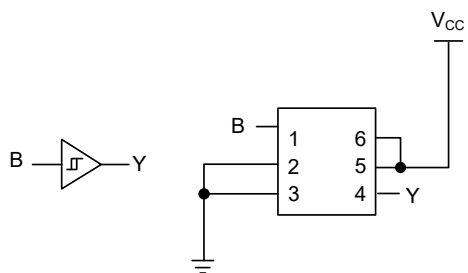


Figure 7. Buffer

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +6.5	V
Input Voltage	V_{IN}		-0.5 ~ +6.5	V
Output Voltage	V_{OUT}	Output in the Power-off state	-0.5 ~ +6.5	V
		Output in the High or Low state	-0.5 ~ $V_{CC}+0.5$	V
Continuous V_{CC} or GND Current	I_{CC}		±100	mA
Continuous Output Current	I_{OUT}	$V_{OUT}=0V \sim V_{CC}$	±50	mA
Input Clamp Current	I_{IK}	$V_{IN}<0V$	-50	mA
Output Clamp Current	I_{OK}	$V_{OUT}>V_{CC}$ or $V_{OUT}<0V$	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	High or Low state	0		V_{CC}	V
Ambient Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-Going Input Threshold Voltage	V_{T+}	$V_{CC}=1.65V$	0.79		1.16	V
		$V_{CC}=2.3V$	1.11		1.56	V
		$V_{CC}=3V$	1.5		1.87	V
		$V_{CC}=4.5V$	2.16		2.74	V
		$V_{CC}=5.5V$	2.61		3.33	V
Negative-Going Input Threshold Voltage	V_{T-}	$V_{CC}=1.65V$	0.35		0.62	V
		$V_{CC}=2.3V$	0.58		0.87	V
		$V_{CC}=3V$	0.84		1.19	V
		$V_{CC}=4.5V$	1.41		1.9	V
		$V_{CC}=5.5V$	1.87		2.29	V
Hysteresis Voltage ($V_{T+}-V_{T-}$)	ΔV_T	$V_{CC}=1.65V$	0.3		0.62	V
		$V_{CC}=2.3V$	0.4		0.8	V
		$V_{CC}=3V$	0.53		0.87	V
		$V_{CC}=4.5V$	0.71		1.04	V
		$V_{CC}=5.5V$	0.71		1.11	V
High-Level Output Voltage	V_{OH}	$V_{CC}=1.65 \sim 5.5V, I_{OH}=-100\mu A$	$V_{CC}-0.1$			V
		$V_{CC}=1.65V, I_{OH}=-4mA$	1.2			V
		$V_{CC}=2.3V, I_{OH}=-8mA$	1.9			V
		$V_{CC}=3.0V, I_{OH}=-16mA$	2.4			V
		$I_{OH}=-24mA$	2.3			V
		$V_{CC}=4.5V, I_{OH}=-32mA$	3.8			V
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65 \sim 5.5V, I_{OL}=100\mu A$			0.1	V
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	V
		$V_{CC}=2.3V, I_{OL}=8mA$			0.3	V
		$V_{CC}=3.0V, I_{OL}=16mA$			0.4	V
		$I_{OL}=24mA$			0.55	V
		$V_{CC}=4.5V, I_{OL}=32mA$			0.55	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0 \sim 5.5V$, $V_{IN}=5.5V$ or GND			± 1	μA
Power OFF Leakage Current	I_{off}	$V_{CC}=0V$, V_{IN} or $V_{OUT}=5.5V$			± 10	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=1.65 \sim 5.5V$, $V_{IN}=5.5V$ or GND, $I_{OUT}=0A$			10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=3 \sim 5.5V$, One input at $V_{CC}-0.6V$, Other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_I	$V_{CC}=3.3V$, $V_{IN}=V_{CC}$ or GND		3.5		pF

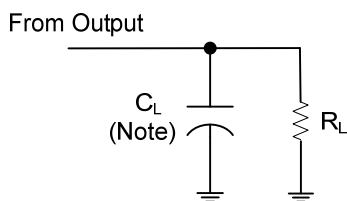
■ SWITCHING CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PD}	$V_{CC}=1.8\pm 0.15V$, $C_L=30pF$, $R_L=1k\Omega$	3.2		14.4	ns
		$V_{CC}=2.5\pm 0.2V$, $C_L=30pF$, $R_L=500\Omega$	2		8.3	ns
		$V_{CC}=3.3\pm 0.3V$, $C_L=50pF$, $R_L=500\Omega$	1.5		6.3	ns
		$V_{CC}=5\pm 0.5V$, $C_L=50pF$, $R_L=500\Omega$	1.1		5.1	ns

■ OPERATING CHARACTERISTICS ($f=10MHz$, $T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC}=1.8V$		20		pF
		$V_{CC}=2.5V$		20		pF
		$V_{CC}=3.3V$		21		pF
		$V_{CC}=5V$		22		pF

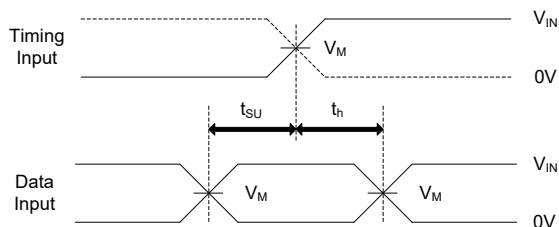
■ TEST CIRCUIT AND WAVEFORMS



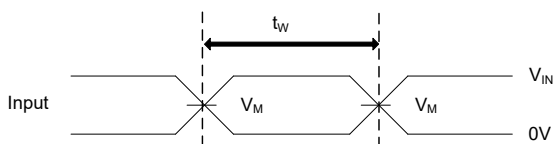
TEST CIRCUIT

Note: C_L includes probe and jig capacitance.

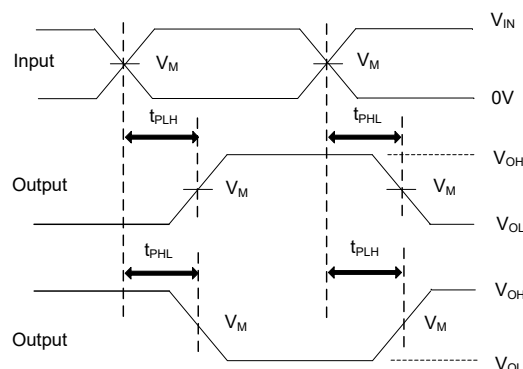
V_{CC}	Inputs		V_M	C_L	R_L
	V_{IN}	t_R, t_F			
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	1K Ω
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	500 Ω
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	50pF	500 Ω
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	50pF	500 Ω



SETUP TIME AND HOLD TIME



PULSE WIDTH



PROPAGATION DELAY TIMES

Not

es: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_O = 50\Omega$.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.