



U74LVC1G74

CMOS IC

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

DESCRIPTION

This single positive-edge-triggered D-type flip-flop is designed for 1.65V to 5.5V V_{CC} operation.

A low level at the preset($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs .when $\overline{PRE}$ and $\overline{CLR}$ are inactive(high),data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FEATURES

- * Supports 5V V_{CC} operation
- * Inputs accept voltages to 5.5V
- * Max t_{pd} of 5.9ns at 3.3V
- * Typical $V_{OLP} < 0.8V$ at $V_{CC} = 3.3V$, $T_A = 25^\circ C$
- * Typical $V_{OHV} > 2V$ at $V_{CC} = 3.3V$, $T_A = 25^\circ C$
- * Low Power Consumption, $I_{CC} = 10\mu A$ (Max.)
- * I_{OFF} Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection

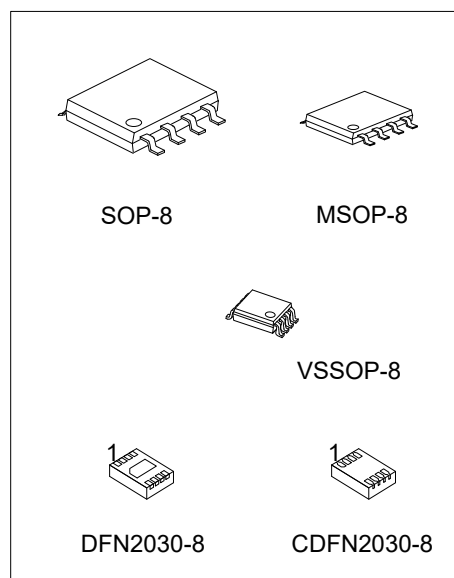
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC1G74L-S08-R	U74LVC1G74G-S08-R	SOP-8	Tape Reel
U74LVC1G74L-SM1-R	U74LVC1G74G-SM1-R	MSOP-8	Tape Reel
U74LVC1G74L-V08-R	U74LVC1G74G-V08-R	VSSOP-8	Tape Reel
U74LVC1G74L-K08-2030-R	U74LVC1G74G-K08-2030-R	DFN2030-8	Tape Reel
U74LVC1G74L-CK08-2030-R	U74LVC1G74G-CK08-2030-R	CDFN2030-8	Tape Reel

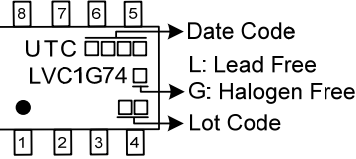
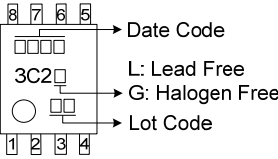
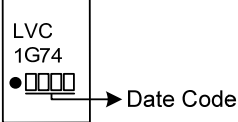
U74LVC1G74G-S08-R

- (1) Packing Type
(2) Package Type
(3) Green Package

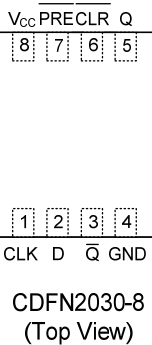
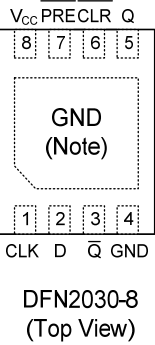
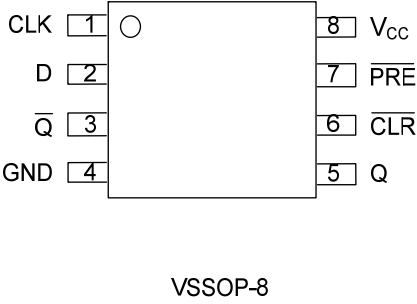
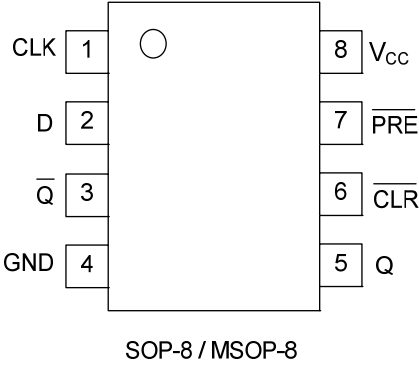
- (1) R: Tape Reel
(2) S08: SOP-8, K08-2030: DFN2030-8
SM1: MSOP-8, V08: VSSOP-8
CK08-2030: CDFN2030-8
(3) G: Halogen Free and Lead Free, L: Lead Free



MARKING

SOP-8 / MSOP-8	VSSOP-8
	
DFN2030-8 / CDFN2030-8	-
	-

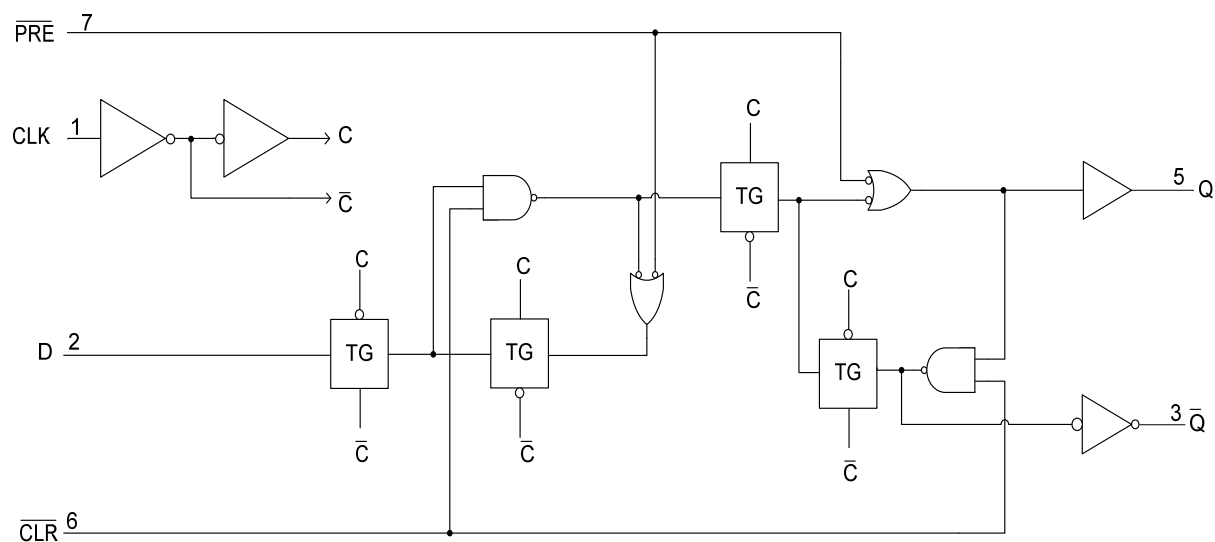
PIN CONFIGURATION



Note: Connect exposed pad to GND.

INPUTS				OUTPUT	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q_0}$

■ **LOGIC DIAGRAM** (positive logic)



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 6.5	V
Input Voltage	V_{IN}	-0.5 ~ 6.5	V
Voltage range applied to any output in the high-impedance or power-off state	V_{OUT}	-0.5 ~ 6.5	V
Voltage range applied to any output in the high or low state	V_{OUT}	-0.5 ~ $V_{CC}+0.5$	V
Input Clamp Current($V_{IN}<0$)	I_{IK}	-50	mA
Output Clamp Current($V_{OUT}<0$)	I_{OK}	-50	mA
Output Current	I_{OUT}	± 50	mA
V_{CC} or GND Current	I_{CC}	± 100	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		1.65		5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=1.8V\pm 0.15V$, $2.5V\pm 0.2V$			20	ns/V
		$V_{CC}=3.3V\pm 0.3V$			10	ns/V
		$V_{CC}=5V\pm 0.5V$			5	ns/V
Operating Temperature	T_A		-40		+125	°C

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ STATIC CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^\circ\text{C}$			$T_A=-40\sim+125^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-level input voltage	V_{IH}	$V_{CC}=1.65V$ to $1.95V$	$0.65\times V_{CC}$				$0.65\times V_{CC}$		V
		$V_{CC}=2.3V$ to $2.7V$	1.7				1.7		V
		$V_{CC}=3V$ to $3.6V$	2				2		V
		$V_{CC}=4.5V$ to $5.5V$	$0.7\times V_{CC}$				$0.7\times V_{CC}$		V
Low-level input voltage	V_{IL}	$V_{CC}=1.65V$ to $1.95V$			$0.35\times V_{CC}$			$0.35\times V_{CC}$	V
		$V_{CC}=2.3V$ to $2.7V$			0.7			0.7	V
		$V_{CC}=3V$ to $3.6V$			0.8			0.8	V
		$V_{CC}=4.5V$ to $5.5V$			$0.3\times V_{CC}$			$0.3\times V_{CC}$	V
High-level Output Current	I_{OH}	$V_{CC}=1.65V$			-4			-4	mA
		$V_{CC}=2.3V$			-8			-8	mA
		$V_{CC}=3V$			-16			-16	mA
		$V_{CC}=4.5V$			-24			-24	mA
					-32			-32	mA

■ STATIC CHARACTERISTICS (Cont.)

(All typical values are at $V_{CC}=3.3V$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^{\circ}C$			$T_A=-40\sim+125^{\circ}C$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Low-level Output Current	I_{OL}	$V_{CC}=1.65V$			4			4	mA
		$V_{CC}=2.3V$			8			8	mA
		$V_{CC}=3V$			16			16	mA
					24			24	mA
		$V_{CC}=4.5V$			32			32	mA
High-Level Output Voltage	V_{OH}	$V_{CC}=1.65V$ to $5.5V$, $I_{OH}=-100\mu A$	$V_{CC}-0.1$			$V_{CC}-0.1$			V
		$V_{CC}=1.65V$, $I_{OH}=-4mA$	1.2			0.95			V
		$V_{CC}=2.3V$, $I_{OH}=-8mA$	1.9			1.7			V
		$V_{CC}=3V$							
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65V$ to $5.5V$, $I_{OL}=100\mu A$			0.1			0.1	V
		$V_{CC}=1.65V$, $I_{OL}=4mA$			0.45			0.7	V
		$V_{CC}=2.3V$, $I_{OL}=8mA$			0.3			0.45	V
		$V_{CC}=3V$			0.4			0.6	V
					0.55			0.8	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0V \sim 5.5V$, $V_{IN}=5.5V$ or GND			± 5			± 5	μA
		$V_{CC}=0V$, V_{IN} or $V_{OUT}=5.5V$			± 10			± 10	μA
		$V_{CC}=1.65V$ to $5.5V$, $V_{IN}=5.5V$ or GND $I_{OUT}=0$			10			10	μA
		$V_{CC}=3V$ to $5.5V$, One input at $V_{CC}-0.6V$, Other inputs at V_{CC} or GND			500			500	μA

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^{\circ}C$			$T_A=-40\sim+125^{\circ}C$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Clock frequency	f_{clock}	$V_{CC}=1.8V$			60			55	MHz
		$V_{CC}=2.5V$			105			85	MHz
		$V_{CC}=3.3V$			120			95	MHz
		$V_{CC}=5.0V$			160			120	MHz
Pulse duration	t_w	$V_{CC}=1.8V$	CLK	6.2		6.2			ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	6.2		6.2			ns
		$V_{CC}=2.5V$	CLK	2.7		2.7			ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	2.7		2.7			ns
		$V_{CC}=3.3V$	CLK	2.7		2.7			ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	2.7		2.7			ns
		$V_{CC}=5.0V$	$\overline{PRE}$ or $\overline{CLR}$ Low	2		2			ns
				2		2			ns

■ TIMING REQUIREMENTS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Setup time before CLK↑ from Data to $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	t _{su}	V _{CC} =1.8V	CLK		2.9			2.9	ns
			$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Low		1.9			1.9	ns
		V _{CC} =2.5V	CLK		1.7			1.7	ns
			$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Low		1.4			1.4	ns
		V _{CC} =3.3V	CLK		1.3			1.3	ns
			$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Low		1.2			1.2	ns
		V _{CC} =5.0V	CLK		1.1			1.1	ns
			$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Low		1			1	ns
		V _{CC} =1.8V			0			0	ns
		V _{CC} =2.5V			0.3			0.3	ns
Hold time, data after CLK↑	t _h	V _{CC} =3.3V			1.2			1.2	ns
		V _{CC} =5.0V			0.5			0.5	ns

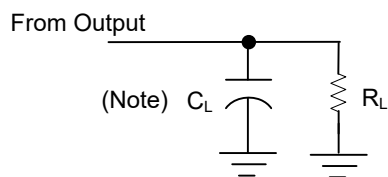
■ SWITCHING CHARACTERISTICS (See Fig. 1 and Fig. 2 for test circuit and waveforms.)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Frequency Response	f _{Max}	V _{CC} =1.8V	60			55			MHz
		V _{CC} =2.5V	105			85			MHz
		V _{CC} =3.3V	120			95			MHz
		V _{CC} =5.0V	160			120			MHz
Propagation delay from input (CLK) to output(Q)	t _{PLH} /t _{PHL}	V _{CC} =1.8V	1.5		15.4	1.5		17.4	ns
		V _{CC} =2.5V	1.0		9.1	1.0		11.1	ns
		V _{CC} =3.3V	1.0		7.9	1.0		9.9	ns
		V _{CC} =5.0V	1.0		6.1	1.0		8.1	ns
Propagation delay from input (CLK) to output($\overline{Q}$)	t _{PLH} /t _{PHL}	V _{CC} =1.8V	1.5		16.4	1.5		18.4	ns
		V _{CC} =2.5V	1.0		9.7	1.0		11.7	ns
		V _{CC} =3.3V	1.0		8.2	1.0		10.2	ns
		V _{CC} =5.0V	1.0		6.4	1.0		8.1	ns
Propagation delay from input ($\overline{\text{PRE}}$ or $\overline{\text{CLR}}$) to output(Q or $\overline{Q}$)	t _{PLH} /t _{PHL}	V _{CC} =1.8V	1.5		14.9	1.5		16.9	ns
		V _{CC} =2.5V	1.0		9	1.0		11	ns
		V _{CC} =3.3V	1.0		7.9	1.0		9.9	ns
		V _{CC} =5.0V	1.0		6.1	1.0		8.1	ns

■ OPERATING CHARACTERISTICS (f=10MHz, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C _{IN}	V _{CC} =3.3V, V _{IN} =V _{CC} or GND		5		pF
Power Dissipation Capacitance	C _{PD}	V _{CC} =1.8V		35		pF
		V _{CC} =2.5V		35		pF
		V _{CC} =3.3V		37		pF
		V _{CC} =5.0V		40		pF

■ TEST CIRCUIT AND WAVEFORMS

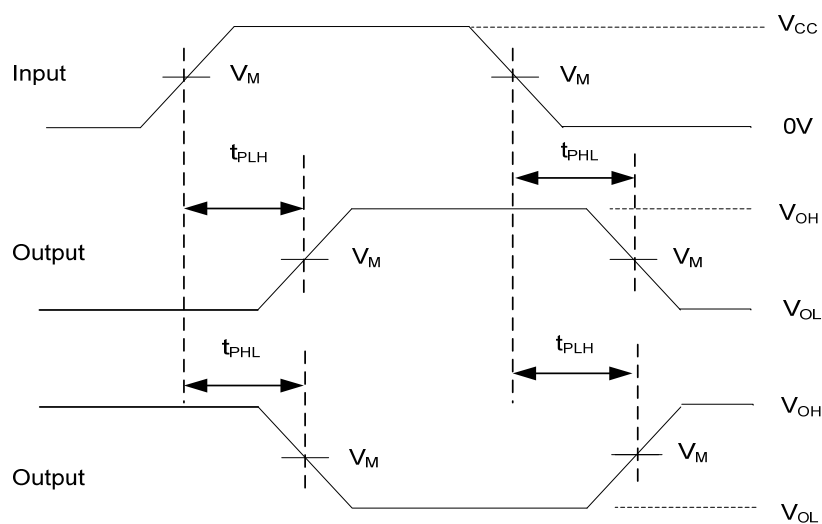


TEST CIRCUIT

Note: C_L includes probe and jig capacitance.

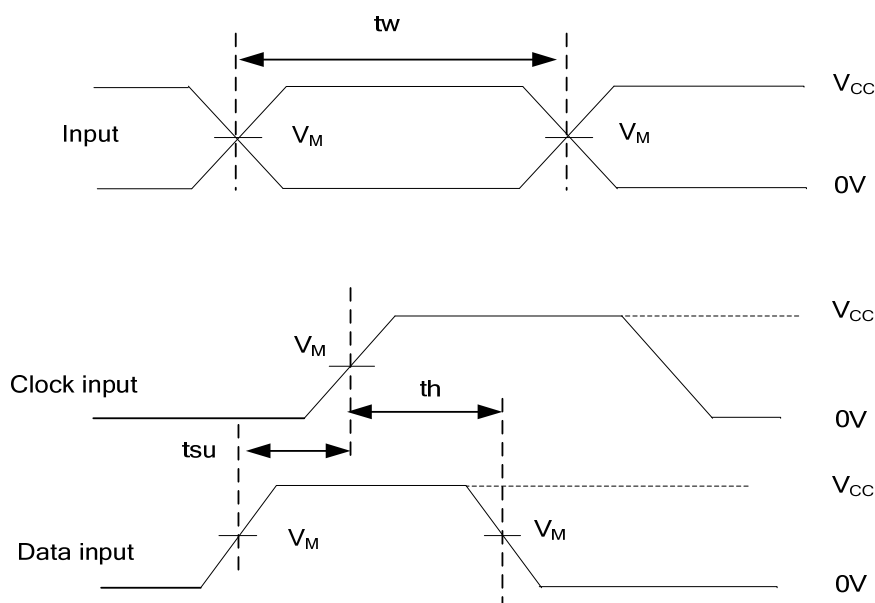
Fig. 1 Load circuitry for switching times.

V_{CC}	Inputs		V_M	C_L	R_L
	V_{IN}	t_R, t_F			
1.8V	V_{CC}	$\leq 2\text{ns}$	$V_{CC}/2$	30pF	1K Ω
2.5V	V_{CC}	$\leq 2\text{ns}$	$V_{CC}/2$	30pF	500 Ω
3.3V	3V	$\leq 2.5\text{ns}$	1.5V	50pF	500 Ω
5V	V_{CC}	$\leq 2.5\text{ns}$	$V_{CC}/2$	50pF	500 Ω



PROPAGATION DELAY TIMES

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



Note: All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 10\text{MHz}$, $Z_O=50\Omega$

Fig. 2 Propagation delay from input to output and input voltage waveforms.

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