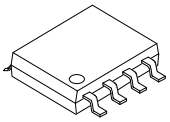
LOW COST POWER-SAVING MODE PWM CONTROLLER FOR FLYBACK CONVERTERS



SOP-8

■ DESCRIPTION

The UTC **UC3800/B** is a high performance current mode PWM controller ideally suited for low standby power. High voltage startup is implemented in UTC **UC3800/B**, which features with short startup time and no standby current. At no load condition, the IC operates in power-saving mode for lower standby power, decreasing frequency for higher conversion efficiency at light load condition.

The internal slope compensation improves system stability at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch, which offering minimal external component count in the design. Excellent EMI performance is achieved with UTC proprietary frequency hopping technique (ZL201020615247.1) together with soft driver control. Audio noise is eliminated due to switch frequency more than 20kHz during operation.

The UTC **UC3800/B** has such applications as: battery charger, power adaptor, set-top box power supplies, ink jet printers, open-frame SMPS.

■ FEATURES

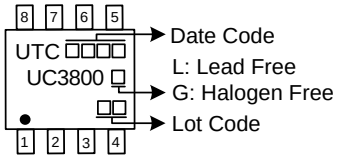
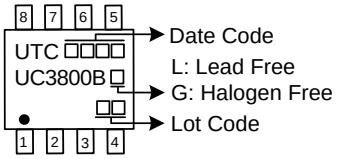
* UTC proprietary frequency hopping technology for Improved EMI performance.
* Power-saving mode for high light-load and standby efficiency
* Soft Start
* Dynamic peak current limiting for constant output power
* Built-in synchronized slope compensation
* OTP,OLP,OVP, LNO-OVP, Brownout and V_{DD} clamp for higher security
* Fixed switch frequency 65kHz
* Gate output voltage clamped at 16V
* Low start-up current
* Cycle-by-cycle Current Limiting
* Under voltage lockout (UVLO)
* Few external components required

■ ORDERING INFORMATION

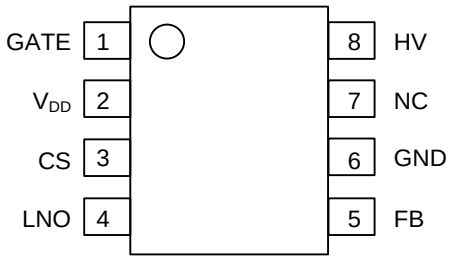
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC3800L-S08-R	UC3800G-S08-R	SOP-8	Tape Reel
UC3800BL-S08-R	UC3800BG-S08-R	SOP-8	Tape Reel

UC3800BG-S08-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

UC3800	UC3800B
	

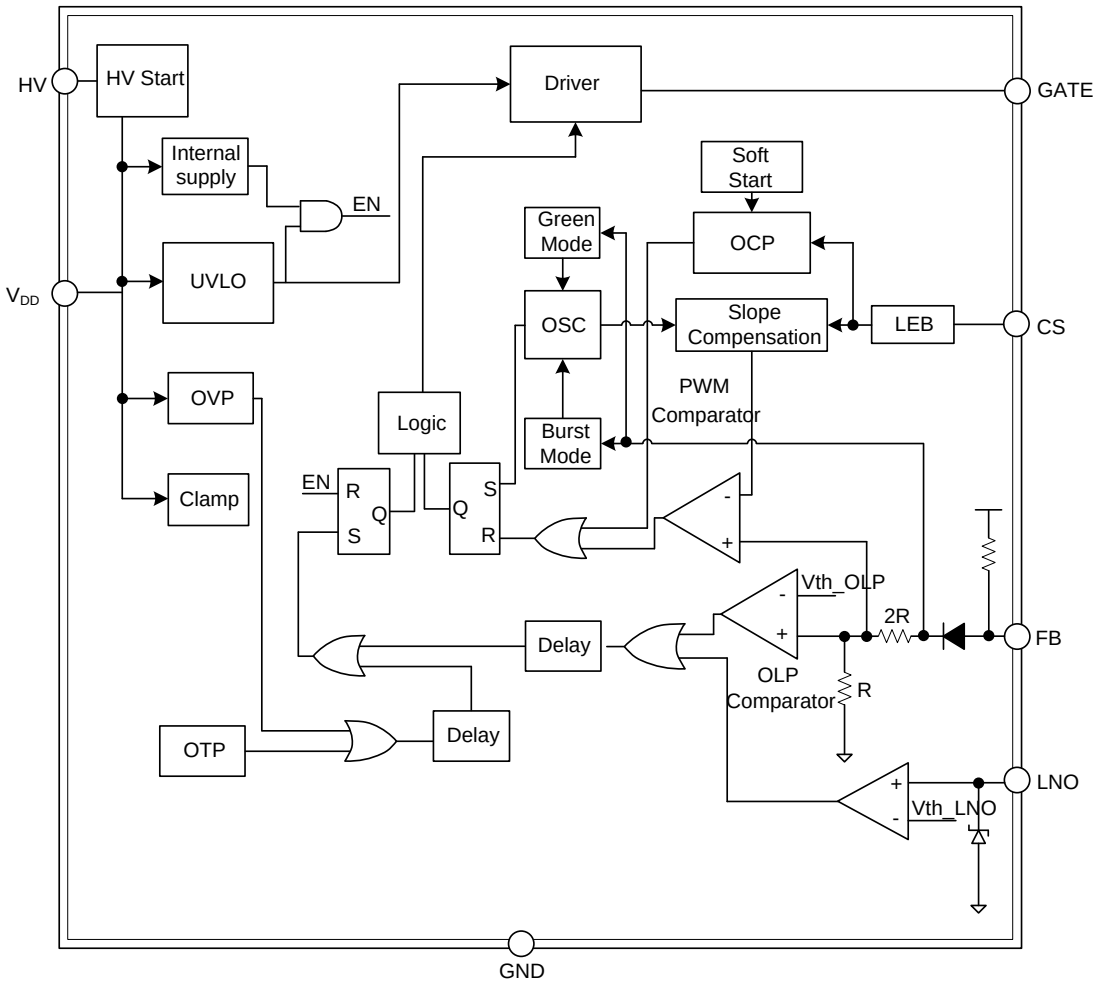
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	PIN TYPE	DESCRIPTION
1	GATE	O	Totem-pole gate driver output for power MOSFET.
2	V_{DD}	P	Supply voltage
3	CS	I	Current sense input.
4	LNO	I	This pin is connected to the line input via two resistors to achieve line voltage over protect function and Brownout
5	FB	I	The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin.
6	GND	P	Ground.
7	NC		
8	HV	I	Connected to the line input or bulk capacitor via resistor for setup.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, V_{DD} =16V, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	30	V
Input Voltage to FB Pin	V_{FB}	-0.3 ~ 6	V
Input Voltage to CS Pin	V_{SENSE}	-0.3 ~ 6	V
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-50 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ OPERATING RANGE

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	9 ~ 24	V

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	150	°C/W

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{DD}=16V，unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION							
Supply current from HV Pin		I_{HV}	HV=100V		0.6		mA
Start Up Current		I_{STR}	V_{DD} = $V_{DD(ON)}$-0.1V		2	15	μA
IC Operating current		I_{OP1}	V_{FB}=3.5V		0.8	1.8	mA
V_{DD} Zener Clamp Voltage		$V_{DD(CLAMP)}$	I_{DD}=20mA	32	34	36	V
UNDER-VOLTAGE LOCKOUT SECTION							
Start Threshold Voltage		$V_{DD(ON)}$		16.5	18.5	21	V
Min. Operating Voltage		$V_{DD(OFF)}$		6	7	8	V
Hysteresis		$V_{DD(HY)}$			6		V
CONTROL SECTION							
V_{FB} Open Loop Voltage Level		$V_{FB-OPEN}$		5.0	5.4		V
PWM Input Gain		A_{VCS}	$\Delta V_{FB}/\Delta V_{CS}$		3		V/V
The FB threshold enter burst mode		$V_{FB(IN)}$	**UC3800**		1.1		V
			UC3800B		0.85		
The FB threshold exit burst mode		$V_{FB(OUT)}$	**UC3800**		1.2		V
			UC3800B		0.9		
Switch Frequency	Normal	F_{SW}	V_{FB}=3.5V, hopping Rang	60	65	70	KHz
	Power-Saving		V_{FB}=1.4V	19			KHz
Duty Cycle		D_{MAX}	V_{FB}=3.5V, V_{SENSE}=0	70	78	85	%
Frequency Hopping		$F_{J(SW)}$		-9		+9	%
Frequency V_{DD} Stability		F_{DV}	V_{DD}=12V~20V			5	%
Frequency Temperature Stability		F_{DT}	T=-40~85°C			10	%
PROTECTION SECTION							
V_{CC} Over Voltage Protection Threshold		V_{OVP}	V_{FB}=3.5V	25	27	29	V
FB PIN Over Load Protection Threshold		V_{OLP}			4.6		V
Over Load Protection Delay-Time		T_{Delay}		60	88	120	mS
Soft start time		T_{SS}			5		mS
OTP Level		T_{OTP}			150		°C

■ ELECTRICAL CHARACTERISTICS (Note.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMITING SECTION						
Peak Current Flat Threshold Voltage	V_{CS-F}	V_{FB}=4V, Duty≥60%		0.97		V
Peak Current Valley Threshold Voltage	V_{CS-V}	V_{FB}=4V, Duty=0%	0.57	0.62	0.67	V
Lead Edge Blanking Time	T_{LEB}			350		ns
DRIVER OUTPUT SECTION						
Output Voltage Low State	V_{OL}	V_{DD}=16V,I_O=-20mA			1	V
Output Voltage High State	V_{OH}	V_{DD}=16V,I_O= 20mA	11			V
Output clamp Voltage	V_Clamping			16		V
Output Voltage Rise Time	t_R	C_L=1.0nF		150		ns
Output Voltage Fall Time	t_F	C_L=1.0nF		60		ns
LNO SECTION						
Threshold voltage for LNO	V_{TH_LNO}		0.93	1.03	1.10	V
Threshold voltage for BNO	V_{TH_BNO}		0.22	0.26	0.30	V

■ OPERATION DESCRIPTION

The UTC **UC3800/B** devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the UTC **UC3800/B** series.

HV Start-up

UTC **UC3800/B** integrated HV start circuit, and provide about 1mA current to charge V_{DD} pin during power on state from HV pin. When V_{DD} cap voltage is higher than UVLO (OFF), the charge current is switched off. At this moment, the V_{DD} capacitor provides current to UTC **UC3800/B** until the auxiliary winding of the main transformer starts to provide the operation current.

Power-Saving Mode Operation

The proprietary Power-Saving Mode function provides linearly decreasing the switching frequency under light-load conditions for higher efficiency. The feedback voltage, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback voltage dropped below the threshold voltage, the switching frequency starts to decrease. This Power-Saving Mode function dramatically reduces power consumption under light-load conditions. The 22KHz minimum frequency control also eliminates the audio noise at any loading conditions.

At zero load condition, the magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. The UTC **UC3800/B** enter burst mode at standby condition to minimize the switching loss and reduces the standby power consumption. Power supplies using the UTC **UC3800/B** can easily meet even the strictest regulations regarding standby power consumption.

Switch Frequency Set

The maximum switch frequency is fixed to 65KHz. Switch frequency is modulated by output power P_{OUT} during IC operating. At no load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. So lower switch frequency at lower load, which more and more improve IC's efficiency at light load. At from no load to light load condition, The IC will operate at from Burst mode to Reducing Frequency Mode. The relation curve between f_{SW} and $P_{OUT}/P_{OUT\ (MAX)}$ as followed Fig.1.

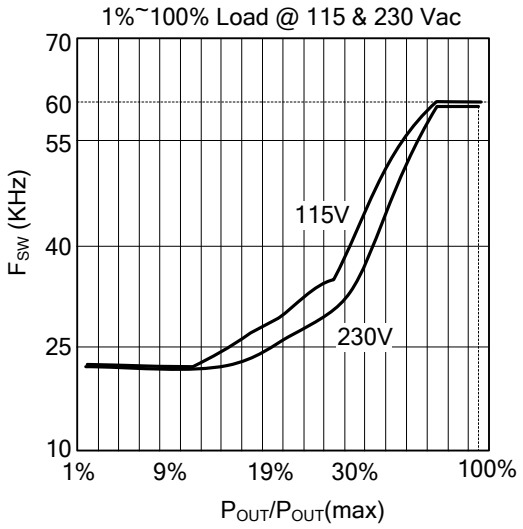


Fig.1 The relation curve between f_{SW} and relative output power P_{OUT}/ $P_{OUT\ (MAX)}$

■ OPERATION DESCRIPTION (Cont.)

Frequency Hopping For EMI Improvement

The Frequency hopping is implemented in the IC; there are two oscillators built-in the IC. The first oscillator is to set the normal switching frequency; the switching frequency is modulated with a period signal generated by the 2nd oscillator. The relation between the first oscillator and the 2nd oscillator as followed Fig.2. So the tone energy is evenly spread out, the spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

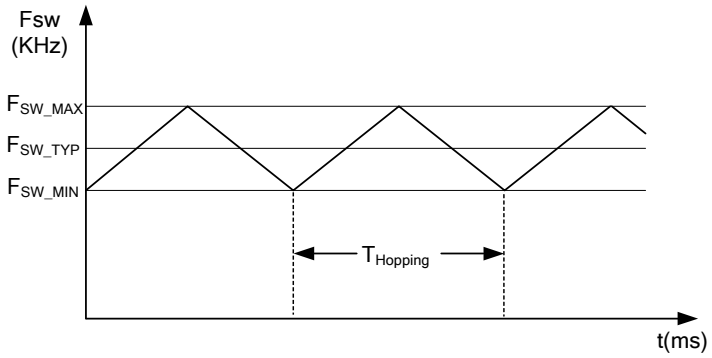


Fig.2 Frequency Hopping

Built-in Slope Compensation

Built-in slope compensation circuit greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation.

Leading-Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a 350ns leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Constant Output Power Limit

When the SENSE voltage, across the sense resistor R_S, reaches the threshold voltage, around 0.95V, the output GATE drive will be turned off after a small propagation delay t_D. This propagation delay will introduce an additional current proportional to $t_D \times V_{IN}/Lp$. Since the propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltage will result in a larger additional current and hence the output power limit is also higher than that under low input line voltage. To compensate this variation for wide AC input range, the threshold voltage is adjusted by the V_{IN} current. Since V_{IN} pin is connected to the rectified input line voltage through a resistor R_{VIN}, a higher line voltage will generate higher V_{IN} current into the V_{IN} pin. The threshold voltage is decreased if the V_{IN} current is increased. Smaller threshold voltage, forces the output GATE drive to terminate earlier, thus reduce the total PWM turn-on time and make the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for wide AC input voltage from 90VAC to 264VAC.

Under Voltage Lockout (UVLO)

The turn-on and turn-off thresholds of the UTC **UC3800/B** are fixed internally at $V_{THD(ON)}/V_{DD(MIN)}$ During start-up, the hold-up capacitor must be charged to $V_{THD(ON)}$ through the start-up resistor, so that the UTC **UC3800/B** will be enabled. The hold-up capacitor will continue to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below $V_{DD(MIN)}$ during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor will be adequate to supply V_{DD} during start-up.

Gate Output

The UTC **UC3800/B** output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. A good tradeoff is achieved through dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 16V clamp is added for MOSFET gate protection at higher than expected V_{DD} input.

■ OPERATION DESCRIPTION (Cont.)

Protection Controls

The IC takes on more protection functions such as OVP, OLP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. Driver is reset after failure is eliminated.

OVP

The OVP will shut down the switching of the power MOSFET whenever V_{DD} >V_{OVP}. The OVP event as followed Fig.3.

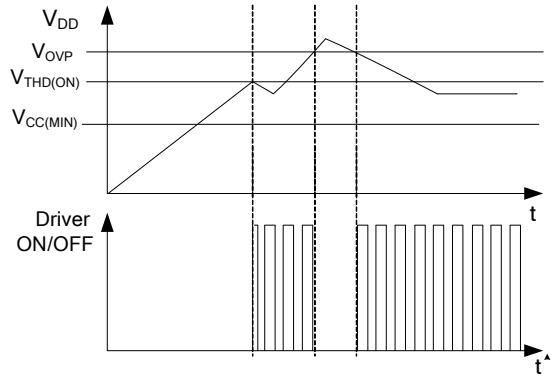


Fig.3 OVP case

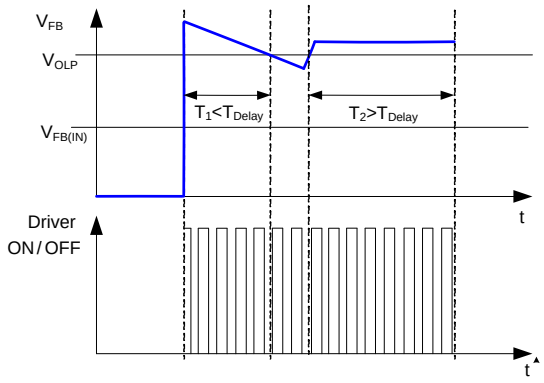


Fig.4 OLP case

OLP

OLP will shut down driver when V_{FB}> V_{OLP} for continual time. The OLP event as followed Fig.4.

LNO-OVP and BNO

LNO will shut down driver when LNO> V_{TH_LNO} or LNO<V_{TH_BNO} for continual time.

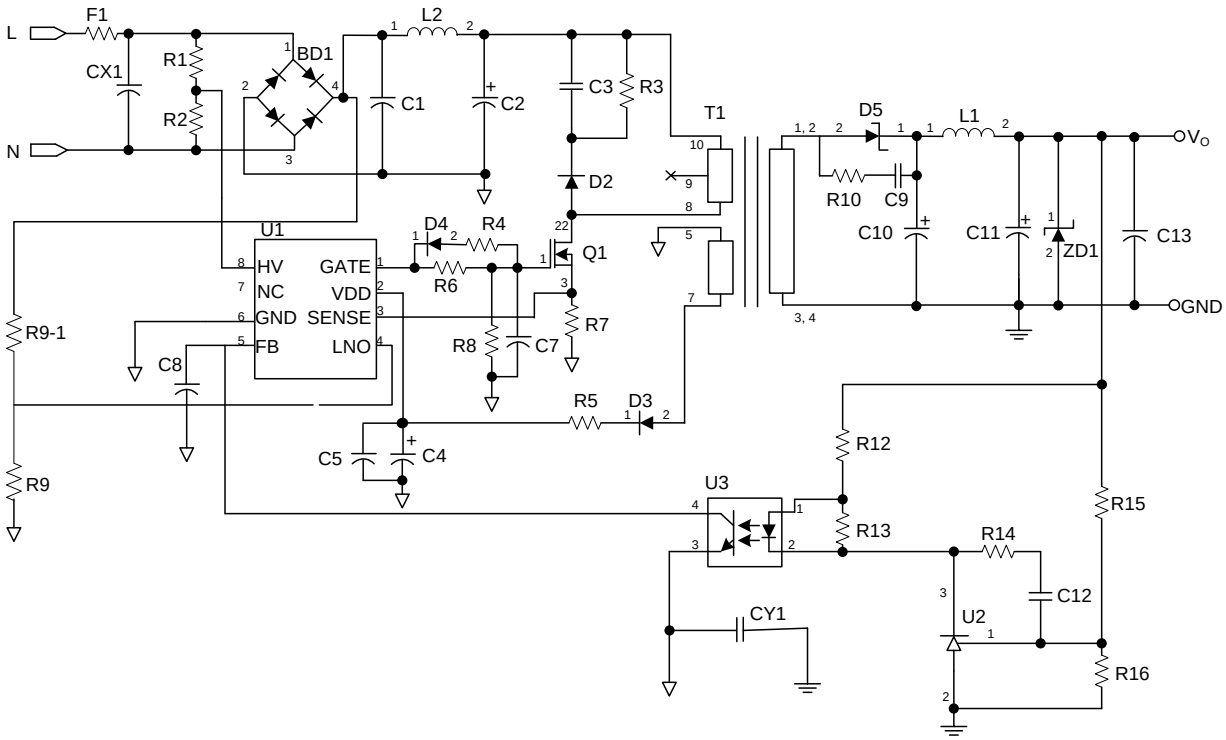
OTP

The internal OTP circuit is implemented to detect the Temperature. As soon as the Temperature is higher than the 150°C, the driver will shut down.

PCB Layout Note

Noise from the current sense or the control signal can cause significant pulse width jitter in continuous-conduction mode, and slope compensation helps alleviate these problems. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the UTC **UC3800/B**, and increasing the power MOS gate resistance is advised.

■ REFRENCE CIRCUIT (12V/1.5A)



BOM

Reference	Component	Reference	Component
BD1	BD 1A/600V	L2	20mH 6*8mm
CX1 (Optional)	NC	Q1	4N60
CY1 (Optional)	YC 220P/400V (Y1)	R1,R2	R 1MΩ 1206
C2	EC 22μF/400V 105°C	R3	R 30KΩ 1206
C1	EC 10μF/400V 105°C	R4 (Optional)	R 20Ω 1W
C3	CC 0.01μF/1000V	R5	R 0Ω 1206
C4	EC 3.3μF/50V	R6	R 100Ω 1206
C5,C13 (Optional)	CC 104P/25V 0805	R7	R 1.1Ω 1W
C7 (Optional)	CC 102P/25V 1206	R8	R 10kΩ 1206
C8	CC 102P/25V 1206	R9/R9-1	R 2.8kΩ / 1MΩ
C9	CC 222P/100V 1206	R10	R 51Ω 0.5W
C10	EC 470u/16V 105°C	R12	R 510Ω 0805
C11	EC 220u/16V 105°C	R13	R 2KΩ 0805
C12	CC 222P/16V 0805	R14	R 0Ω 0805
C14	NC	R15	R 43kΩ 0805
D2	Diode FR107	R16	R 12kΩ 0805
D3	Diode FR102	R17	R 120kΩ 0805
D4 (Optional)		T1	EF-20
D5	Diode SB360	U1	IC **UC3800/B**
F1	R1Ω/0.5W	U2	TL431
L1	10μH 6mm	U3	PC817