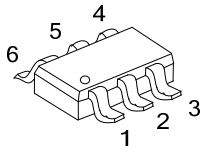
LOW COST POWER-SAVING MODE PWM CONTROLLER FOR FLYBACK CONVERTERS



SOT-26

■ DESCRIPTION

The UTC **UC3856** is a high performance current mode PWM controller ideally suited for low standby power. An externally JFET's gate pin is connected the ST pin, It can achieve HV start, and when start was overed, it is no long consume current to depress the power off. Low V_{DD} startup current make the power reliable on startup design and a large value resistor could be used in the startup circuit to minimize the standby power. At no load condition, the IC operates in power-saving mode for lower standby power, decreasing frequency for Higher conversion efficiency at light load condition.

The UTC **UC3856** contains protection with automatic recovery including OLP (over load protection), OTP (over temperature protection), OVP (over voltage protection), UVLO (V_{DD} over voltage clamp and under voltage lockout).To protect the power MOSFET, Gate-drive output is fixed up to 15V max. The UTC **UC3856** contains protection OCP (cycle-by-cycle current limiting).

The internal slope compensation improves system stability at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch, which offering minimal external component count in the design. Excellent EMI performance is achieved with UTC proprietary frequency hopping technique (ZL201020615247.1) together with soft driver control. Audio noise is eliminated due to switch frequency more than 20kHz during operation.

The UTC **UC3856** has such applications as: battery charger, power adaptor, set-top box power supplies, ink jet printers, open-frame SMPS.

■ FEATURES

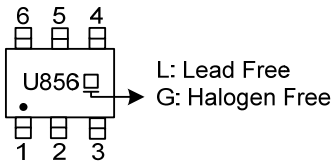
* UTC proprietary frequency hopping technology for Improved EMI performance.
* Power-saving mode for high light-load and standby efficiency
* Dynamic peak current limiting for constant output power
* Built-in synchronized slope compensation
* OTP,OLP,OVP and V_{DD} clamp for higher security
* High efficiency HV start
* Gate output voltage clamped at 15V
* Low start-up current
* Cycle-by-cycle current limiting
* Under voltage lockout (UVLO)
* Few external components required

■ ORDERING INFORMATION

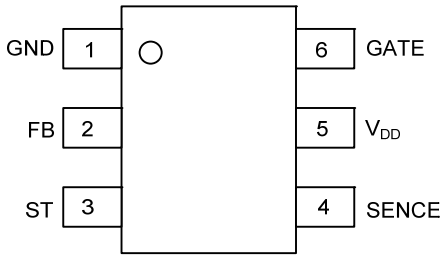
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC3856L-AG6-R	UC3856G-AG6-R	SOT-26	Tape Reel

UC3873AG-AG6-R (1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) AG6: SOT-26 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



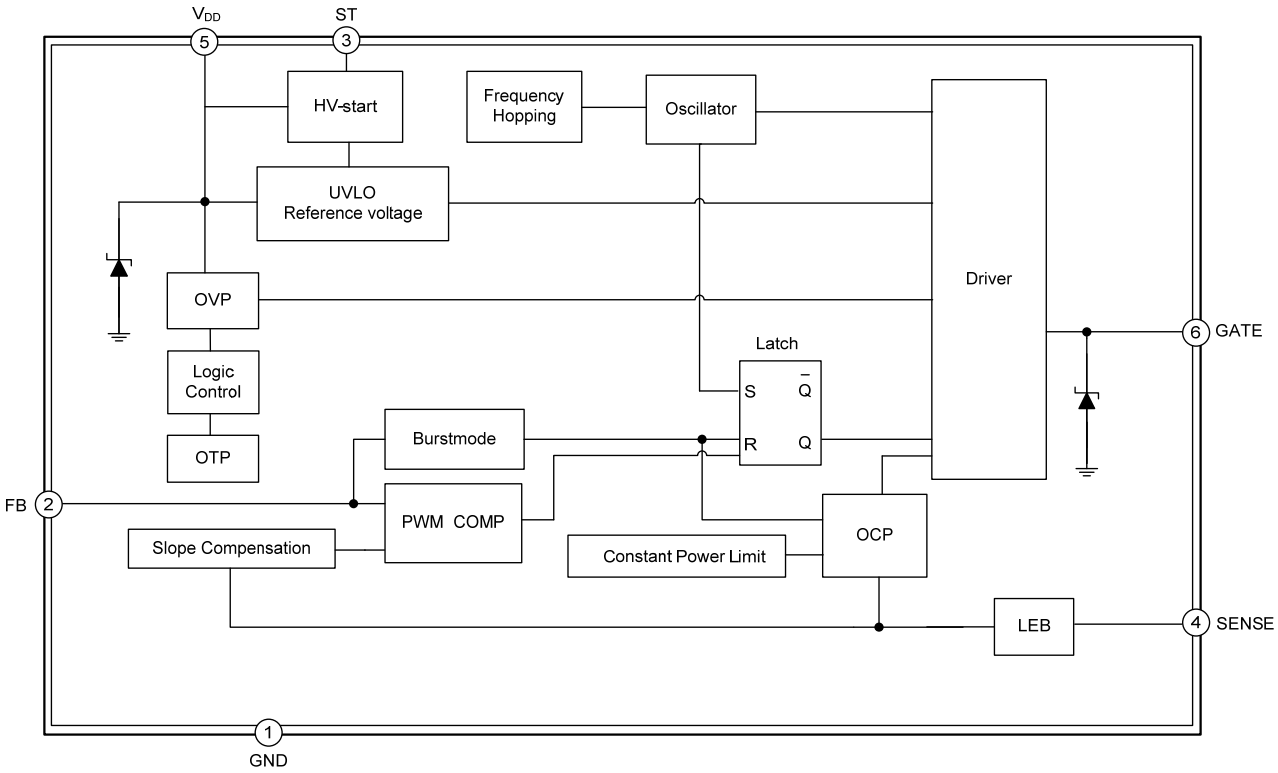
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	PIN TYPE	DESCRIPTION
1	GND	P	Ground.
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input.
3	ST	I	Connected to the line input or bulk capacitor via UF601 for startup.
4	SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
5	V_{DD}	P	Power supply.
6	GATE	O	The totem-pole output driver for driving the power MOSFET.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, V_{DD} =15V, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	35	V
Input Voltage to FB Pin	V_{FB}	-0.3 ~ 7	V
Input Voltage to CS Pin	V_{SENSE}	-0.3 ~ 7	V
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-50 ~ +150	°C

Notes: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ OPERATING RANGE

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	10 ~ 24	V

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{DD}=15V, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HV START							
Supply Current from ST Pin		I_{ST}			0.75		mA
Start Pin Leakage Current After Startup		I_{EAKAGE}				10	μA
SUPPLY SECTION							
Start Up Current		I_{STR}	V_{DD}=$V_{DD(ON)}$-0.5V		2	15	μA
IC Operating current		I_{OP}	V_{FB}=3.5V		0.8	1.8	mA
Start Threshold Voltage		$V_{THD(ON)}$		17	19	21	V
Min. Operating Voltage		$V_{DD(MIN)}$		6	7	8	V
V_{DD} Over Voltage Protection		V_{DD_CLAMP}	$I_{\_CLAMP}$=20mA	31	33	35	V
CONTROL SECTION							
V_{FB} Open Loop Voltage Level		$V_{FB-OPEN}$			5.4		V
PWM Input Gain		A_{VCS}	$\Delta V_{FB}/\Delta V_{CS}$		3		V/V
Burst-Mode Out FB Voltage		$V_{FB(OUT)}$	V_{SENSE} =0		1.5		V
Burst-Mode Enter FB Voltage		$V_{FB(IN)}$	V_{SENSE} =0		1.35		V
Switch Frequency	Normal	F_{SW}	V_{FB}=3.5V	60	65	70	KHz
	Power-Saving		Before enter burst mode	20			KHz
Duty Cycle		D_{MAX}	V_{FB}=3.5V, V_{SENSE}=0	70	78	90	%
Frequency Hopping		$F_{J(SW)}$		-9		+9	%
Frequency VDD Stability		F_{DV}	V_{DD}=12V~20V			10	%
Frequency Temperature Stability		F_{DT}	T=-40~110°C			10	%
PROTECTION SECTION							
V_{CC} Over Voltage Protection Threshold		V_{OVP}		25	27	29	V
FB PIN Over Load Protection Threshold		V_{OLP}			4.2		V
Over Load Protection Delay-Time		T_{Delay}	V_{FB}=3~5V (OLP)	60	88	120	mS
OTP threshold		$T_{(THR)}$			150		°C
CURRENT LIMITING SECTION							
Peak Current Flat Threshold Voltage		V_{CS-F}			0.92		V
Peak Current Valley Threshold Voltage		V_{CS-V}	V_{FB}=4.0V, Duty=0%	0.60	0.65	0.70	V
Lead Edge Blanking Time		T_{LEB}		200	350	550	ns
Soft Start Time		SST			5		ms
DRIVER OUTPUT SECTION							
Output Voltage Low State		V_{OL}	V_{DD}=16,I_O=-20mA			1	V
Output Voltage High State		V_{OH}	V_{DD}=16,I_O=20mA	11			V
Output Voltage Rise Time		t_R	C_L=1.0nF		150		ns
Output Voltage Fall Time		t_F	C_L=1.0nF		60		ns

■ OPERATION DESCRIPTION

The UTC **UC3856** devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the UTC **UC3856** series.

HV Start

A high voltage start pin. An externally JFET's gate pin is connected this pin, It can achieve HV start, and when start was overed, it is no long consume current.

Start-up Current

The start-up current is only 5μA. Low start-up current allows a start-up resistor with a high resistance and a low-wattage to supply the start-up power for the controller. For AC/DC adaptor with universal input range design, a 2.5~3MΩ, 1/8W startup resistor could be used together with a V_{DD} capacitor to provide a fast startup and low power dissipation solution.

Power-Saving Mode Operation

The proprietary Power-Saving Mode function provides linearly decreasing the switching frequency under light-load conditions for higher efficiency. The feedback voltage, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback voltage dropped below the threshold voltage, the switching frequency starts to decrease. This Power-Saving Mode function dramatically reduces power consumption under light-load conditions. The 22KHz minimum frequency control also eliminates the audio noise at any loading conditions.

At zero load condition, the magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. The UTC **UC3856** enter burst mode at standby condition to minimize the switching loss and reduces the standby power consumption. Power supplies using the UTC **UC3856** can easily meet even the strictest regulations regarding standby power consumption.

Switch Frequency Set

The maximum switch frequency is set through the 100KΩ RI-pin resistor to 62KHz. Switch frequency is modulated by output power P_{OUT} during IC operating. At no load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. So lower switch frequency at lower load, which more and more improve IC's efficiency at light load. At from no load to light load condition, The IC will operate at from Burst mode to Reducing Frequency Mode. The relation curve between f_{SW} and $P_{OUT}/P_{OUT\ (MAX)}$ as followed Fig.1. The maximum switch frequency is set through the RI-pin resistor RI: F_{SW}=6200/RI (KΩ) KHz.

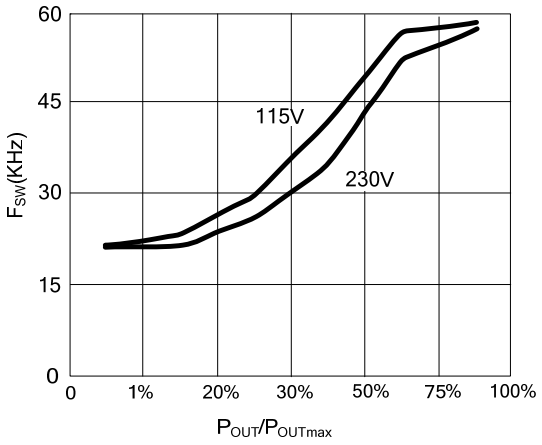


Fig.1 The relation curve between f_{SW} and relative output power P_{OUT}/ $P_{OUT\ (MAX)}$

■ OPERATION DESCRIPTION (Cont.)

Frequency Hopping For EMI Improvement

The Frequency hopping is implemented in the IC; there are two oscillators built-in the IC. The first oscillator is to set the normal switching frequency; the switching frequency is modulated with a period signal generated by the 2nd oscillator. The relation between the first oscillator and the 2nd oscillator as followed Fig.2. So the tone energy is evenly spread out, the spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

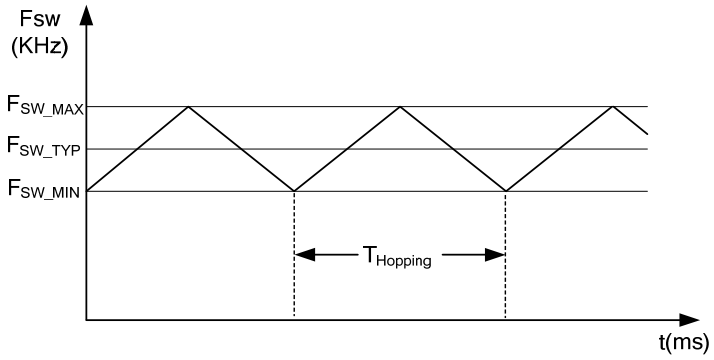


Fig.2 Frequency Hopping

Built-in Slope Compensation

Built-in slope compensation circuit greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation.

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a T_{LEB} leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Constant Output Power Limit

When the SENSE voltage, across the sense resistor R_S, reaches the threshold voltage, around V_{CS-V}, the output GATE drive will be turned off after a small propagation delay t_D. This propagation delay will introduce an additional current proportional to $t_D \times V_{IN}/Lp$. Since the propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltage will result in a larger additional current and hence the output power limit is also higher than that under low input line voltage. To compensate this variation for wide AC input range, the threshold voltage is adjusted by the V_{IN} current. Since V_{IN} pin is connected to the rectified input line voltage through a resistor R_{VIN}, a higher line voltage will generate higher V_{IN} current into the V_{IN} pin. The threshold voltage is decreased if the V_{IN} current is increased. Smaller threshold voltage, forces the output GATE drive to terminate earlier, thus reduce the total PWM turn-on time and make the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for wide AC input voltage from 90VAC to 264VAC.

Under Voltage Lockout (UVLO)

The turn-on and turn-off thresholds of the UTC **UC3856** are fixed internally at $V_{THD(ON)}/V_{DD(MIN)}$. During start-up, the hold-up capacitor must be charged to $V_{THD(ON)}$ through the start-up resistor, so that the UTC **UC3856** will be enabled. The hold-up capacitor will continue to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below $V_{DD(MIN)}$ during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor will be adequate to supply V_{DD} during start-up.

Gate Output

The UTC **UC3856** output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. A good tradeoff is achieved through dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 15V clamp is added for MOSFET gate protection at higher than expected V_{DD} input.

■ OPERATION DESCRIPTION (Cont.)

Protection Controls

The IC takes on more protection functions such as OVP, OLP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. Driver is reset after failure is eliminated.

OVP

The OVP will shut down the switching of the power MOSFET whenever V_{DD} >V_{OVP}. The OVP event as followed Fig.3.

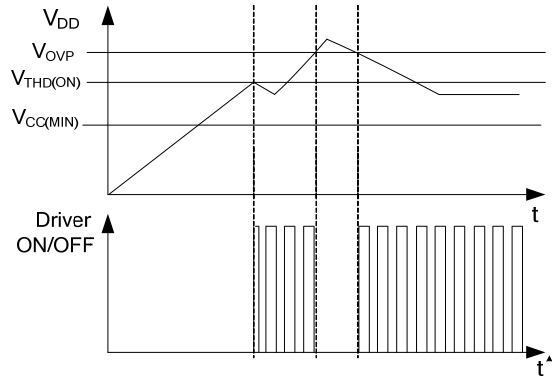


Fig.3 OVP case

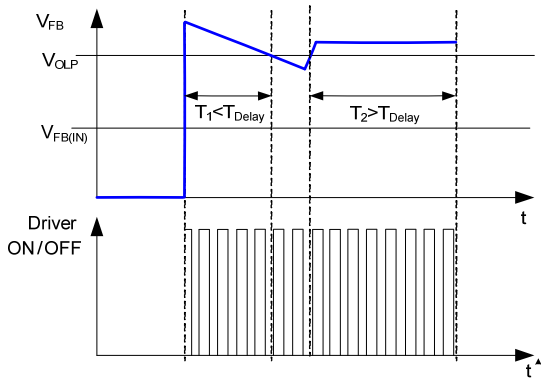


Fig.4 OLP case

OLP

OLP will shut down driver when V_{FB}> V_{OLP} for continual a blanking time. The OLP event as followed Fig.4.

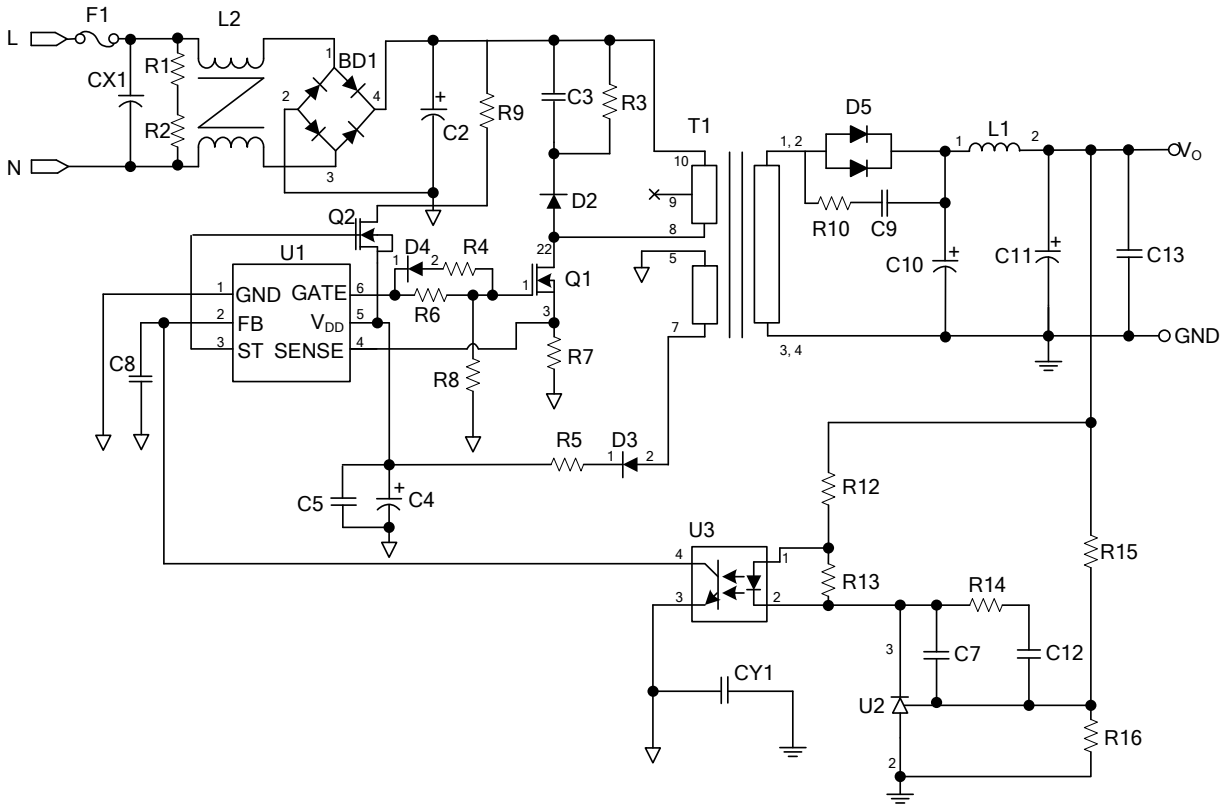
OTP

OTP will shut down driver when junction temperature T_J>$T_{(THR)}$.

PCB Layout Note

Noise from the current sense or the control signal can cause significant pulse width jitter in continuous-conduction mode, and slope compensation helps alleviate these problems. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the UTC **UC3856**, and increasing the power MOS gate resistance is advised.

■ REFRENCE CIRCUIT (12V/2A)

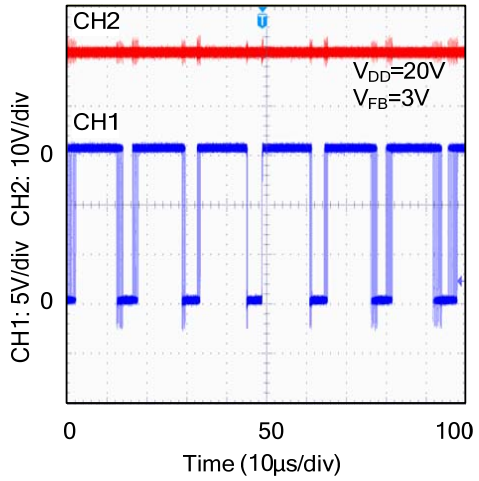


BOM

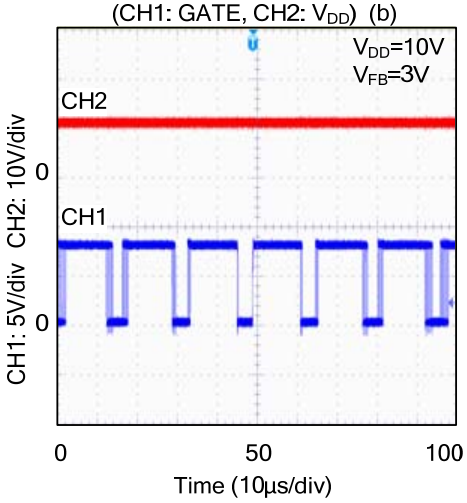
Reference	Component	Reference	Component
BD1	1N4007×4	Q1	4N60
CX1 (Optional)	0.01μF	Q2	UF601
CY1 (Optional)	YC 102P 400V (Y1)	R1	NC
C2	EC 33μF 400V 105°C	R2	NC
C3	CC 0.001μF 1000V	R3	400kΩ1206
C4	EC 10μF 50V	R4 (Optional)	10Ω 0603
C5	CC 1μF 50V	R5	3Ω 0805
C7	10nF 25V	R6	47Ω 0805
C8	CC 1nF 25V	R7	0.66Ω 1W
C9	NC	R8	10kΩ 0603
C10	EC 470μF 25V	R9	100kΩ 1206
C11	EC 220μF 25V	R10	NC
C12	0.1μF/25V 0603	R12	220Ω 0603
C13	0.47μF 1206 50V	R13	1KΩ 0603
D2	Diode 1N4007G	R14	680Ω 0603
D3	BAS21	R15	39kΩ 0603
D4 (Optional)	1N4148	R16	10kΩ 0603
D5	MBR20100C	T1	RM8
F1	2A/250V	U1	IC **UC3856**
L1	NC (Short)	U2	TL431
L2	Choke	U3	PC817

■ TYPICAL CHARACTERISTICS

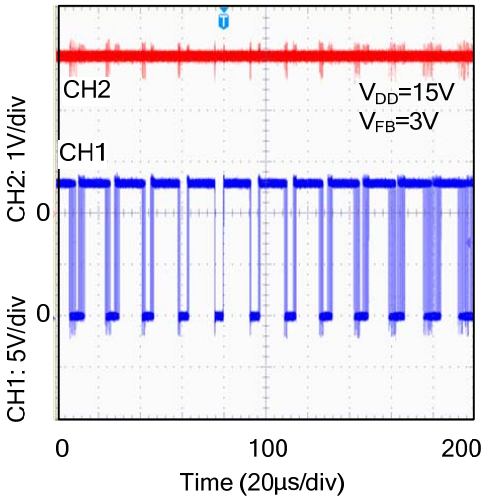
PWM Frequency
(CH1: GATE, CH2: V_{DD}) (a)



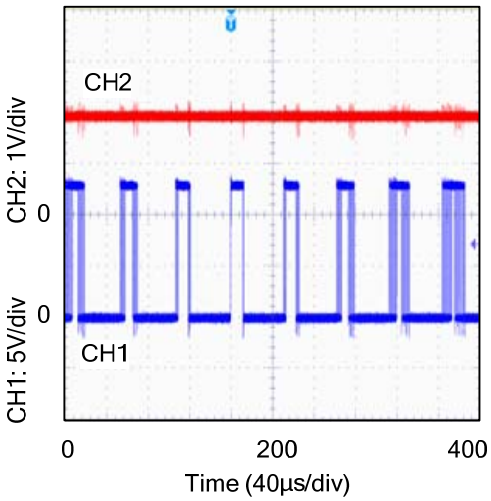
PWM Frequency
(CH1: GATE, CH2: V_{DD}) (b)



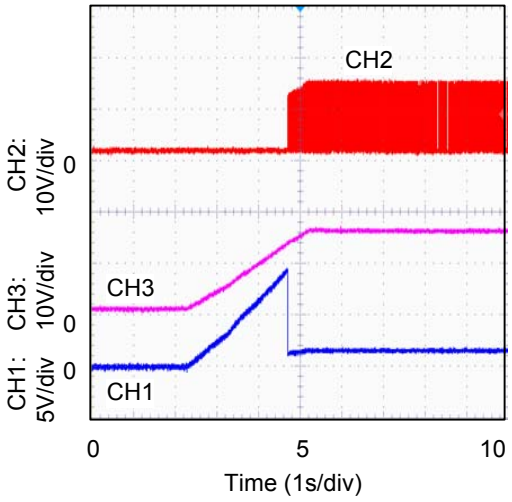
PWM Frequency
(CH1: GATE, CH2: V_{FB}) (c)



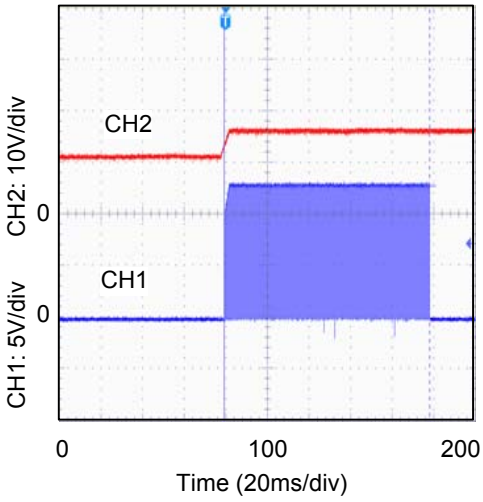
Burst Mode Base Frequency V_{DD}=15V
(CH1: GATE, CH2: V_{FB})



ST PIN
(CH1: ST, CH2: GATE, CH3: V_{DD})



Power Limiting Debounce Time
(CH1: GATE, CH2: V_{DD})



■ TYPICAL CHARACTERISTICS (Cont.)

GATE Drive Output Rising Time/ Falling Time
C_L=1000PF (CH1: GATE)