

**UCD4073B**

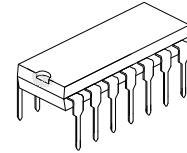
Preliminary

CMOS IC**TRIPLE 3-INPUT AND GATE****DESCRIPTION**

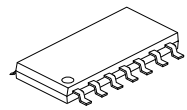
The UTC **UCD4073B** AND gates, provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

FEATURES

- * Supply Voltage Range = 3.0V to 18V
- * All Outputs Buffered
- * Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



DIP-14



SOP-14U

ORDERING INFORMATION

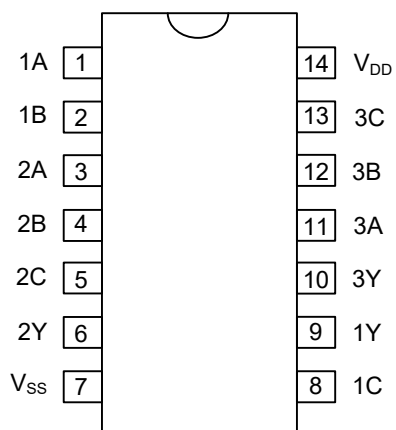
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4073BL-D14-T	UCD4073BG-D14-T	DIP-14	Tube
UCD4073BL-UEA-R	UCD4073BG-UEA-R	SOP-14U	Tape Reel

UCD4024BG-D14-T	
(1) Packing Type	(1) T: Tube, R: Tape Reel
(2) Package Type	(2) D14: DIP-14, UEA: SOP-14U
(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

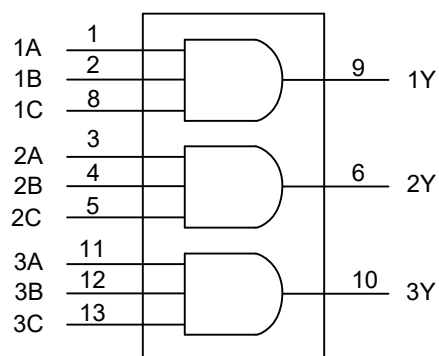
MARKING

DIP-14	SOP-14U
→ Date Code UTC □□□□ UCD4073B□ □□ → Lot Code	→ Date Code UTC □□□□ UCD4073B□ □□ → Lot Code

■ PIN CONFIGURATION



■ LOGIC DIAGRAMS



■ ABSOLUTE MAXIMUM RATING (Voltages Referenced to V_{SS})

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage Range	V_{DD}	-0.5 ~ +18	V
Input or Output Voltage	V_{IN}, V_{OUT}	-0.5 ~ $V_{DD} + 0.5$	V
Input or Output Current	I_{IN}, I_{OUT}	± 10	mA
Operating Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	3 ~ 18	V
Operating Temperature	T_A	-40 ~ +125	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Ambient	θ_{JA}	75 105	°C/W °C/W

■ ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	$V_{DD}=5V$	4.95	5.0		V
		$V_{DD}=10V$	9.95	10		V
		$V_{DD}=15V$	14.95	15		V
Low-Level Output Voltage	V_{OL}	$V_{DD}=5V$		0	0.05	V
		$V_{DD}=10V$		0	0.05	V
		$V_{DD}=15V$		0	0.05	V
High-Level Output Voltage	V_{IH}	$V_{DD}=5V, V_{OUT}=0.5V$ or $4.5V$	3.5	2.75		V
		$V_{DD}=10V, V_{OUT}=1.0V$ or $9.0V$	7.0	5.5		V
		$V_{DD}=15V, V_{OUT}=1.5V$ or $13.5V$	11	8.25		V
Low-Level Output Voltage	V_{IL}	$V_{DD}=5V, V_{OUT}=4.5V$ or $0.5V$		2.25	1.5	V
		$V_{DD}=10V, V_{OUT}=9.0V$ or $1.0V$		4.5	3.0	V
		$V_{DD}=15V, V_{OUT}=13.5V$ or $1.5V$		6.75	4.0	V
High-Level Output Current	I_{OH}	$V_{DD}=5V, V_{OUT}=2.5V$	-1.6	-3.2		mA
		$V_{DD}=5V, V_{OUT}=4.6V$	-0.51	-1		mA
		$V_{DD}=10V, V_{OUT}=9.5V$	-1.3	-2.6		mA
		$V_{DD}=15V, V_{OUT}=13.5V$	-3.4	-6.8		mA
Low-Level Output Current	I_{OL}	$V_{DD}=5V, V_{OUT}=0.4V$	0.51	1		mA
		$V_{DD}=10V, V_{OUT}=0.5V$	1.3	2.6		mA
		$V_{DD}=15V, V_{OUT}=1.5V$	3.4	6.8		mA
Input Current	I_{IN}	$V_{DD}=15V$		± 0.00001	± 0.1	μA
Quiescent Supply Current	I_{DD}	$V_{DD}=5V$		0.01	0.25	μA
		$V_{DD}=10V$		0.01	0.5	μA
		$V_{DD}=15V$		0.02	1.0	μA

Note: I_{OL} and I_{OH} are tested one output at a time.

■ SWITCHING CHARACTERISTICS (Note 1)

($C_L = 50\text{pF}$, $t_R = t_F = 20\text{ns}$, $R_L = 200\text{K}\Omega$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note 2)	MAX	UNIT
Propagation Delay Time	t_{PLH} / t_{PHL}	$V_{DD} = 5\text{V}$		100	300	ns
		$V_{DD} = 10\text{V}$		55	130	ns
		$V_{DD} = 15\text{V}$		45	100	ns
Transition Time	t_{TLH} / t_{THL}	$V_{DD} = 5\text{V}$		100	200	ns
		$V_{DD} = 10\text{V}$		55	100	ns
		$V_{DD} = 15\text{V}$		45	80	ns

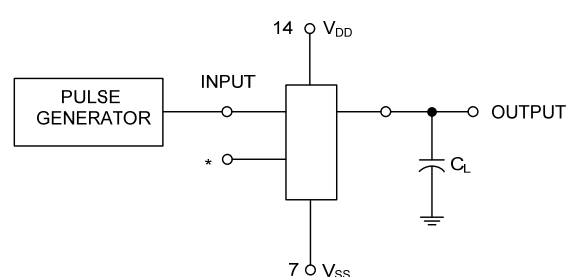
Notes: 1. The formulas given are for the typical characteristics only at 25°C .

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

■ OPERATING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	Any Input.		5	7.5	pF

■ TEST CIRCUIT AND WAVEFORMS



* All unused inputs of AND gate must be connected to V_{DD} .

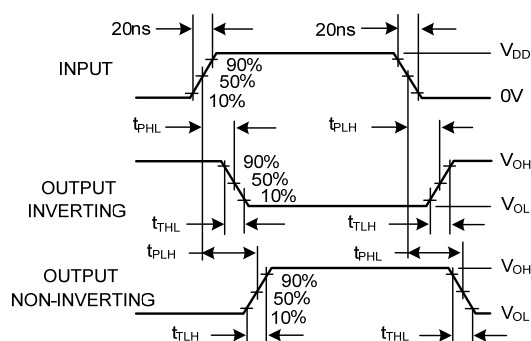
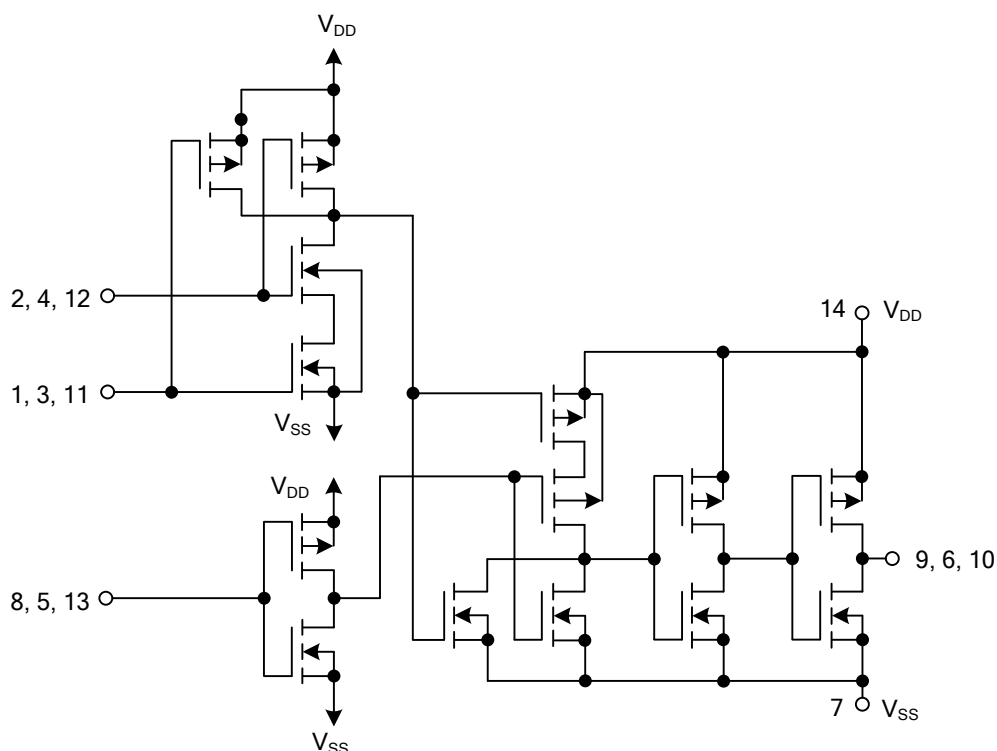


Figure 1. Switching Time Test Circuit and Waveforms

■ TYPICAL APPLICATION CIRCUIT

One of Three Gates Shown



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