



UD18306

LINEAR INTEGRATED CIRCUIT

18V 3A 580KHZ SYNCHRONOUS STEP-DOWN CONVERTER

■ DESCRIPTION

The UTC **UD18306** is an 3A synchronous step-down DC-DC converter with an input voltage range of 4.5V to 18V. The **UD18306** adopts the COT architecture to achieve fast transient responses for high voltage step down applications. The **UD18306** operates in pulse skip mode that maintains high efficiency during light load operation. The **UD18306** features cycle-by-cycle current limit protection and prevent the **UD18306** from the catastrophic damage in output short circuit, over current or inductor saturation. A build-in soft-start block prevents inrush current during start up. The **UD18306** also includes input under-voltage lockout, input over-voltage protection, output under-voltage protection, and over-temperature protection to provide safe and smooth operation in all working conditions.

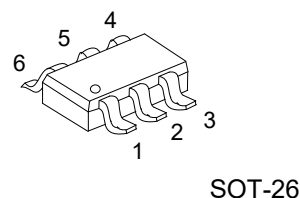
■ FEATURES

- * 4.5V to 18V Input Voltage Range
- * 3A Available Load Current
- * 580kHz Constant Switching Frequency
- * Low $R_{DS(ON)}$ for Internal Switches:
 - High-side: 80m Ω
 - Low-side: 60m Ω
- * Soft Start time: 1.2ms
- * Advanced Constant On-Time Control
- * Fast Transient Responses
- * Input Under-Voltage Lockout
- * Input Over-Voltage Protection
- * Output Under-Voltage Protection
- * Cycle-by-cycle Over Current Limit
- * Short Circuit with Hiccup Mode
- * Over-Temperature Protection
- * Optimized for Low-ESR Ceramic Output Capacitors

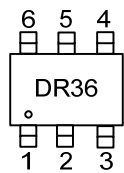
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UD18306L-AG6-R	UD18306G-AG6-R	SOT-26	Tape Reel

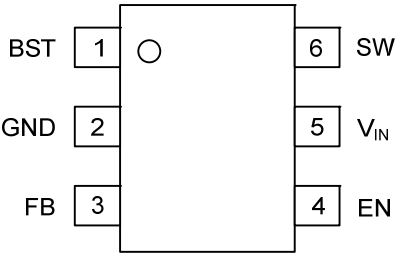
UD18306G-AG6-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) AG6: SOT-26
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



MARKING



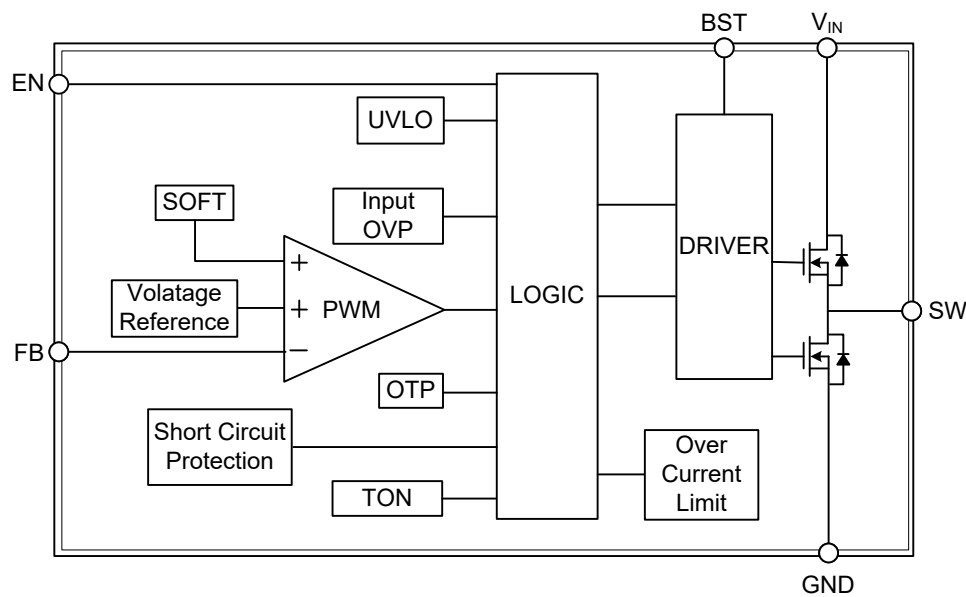
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	PIN	DESCRIPTION
1	BST	P	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1uF ceramic capacitor between this pin and SW pin
2	GND	P	Ground Pin
3	FB	I	Feedback Pin, The device regulates the FB voltage at Feedback Reference Voltage.
4	EN	I	Enable control pin. Pull high to turn on.
5	V _{IN}	P	Supply voltage pin. Decouple this pin to the GND pin with at least a 22μF ceramic capacitor.
6	SW	O	Switch node connection to inductor.

BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (NOTE 2) ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} , EN Voltage		-0.3 ~ 20	V
SW Voltage	V_{SW}	-0.3 ~ 20	V
SW Voltage (Less than 40ns)	V_{SW}	-3 ~ 24	V
BST Voltage	V_{BST}	-0.3 ~ 24	V
BST to SW Voltage		-0.3 ~ 6	V
FB Voltage	V_{FB}	-0.3 ~ 6	V
Operating Junction Temperature	T_J	-40 ~ +160	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-65 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute maximum rating conditions may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (V_{IN})	V_{IN}	4.5 ~ 18	V
Ambient Temperature Range	T_A	-40 ~ +85	$^{\circ}\text{C}$
Operation junction Temperature Range	T_J	-40 ~ +125	$^{\circ}\text{C}$

Note: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + P_D \times R.$$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	100	$^{\circ}\text{C/W}$

■ ELECTRICAL CHARACTERISTICS ($V_{IN}=12V$, $V_{OUT}=3.3V$, $T_A=25^{\circ}C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL SECTION						
Input Voltage Range	V_{IN}		4.5		18	V
Quiescent Current	I_Q	$V_{FB}=0.65V$, SW Open		280		μA
Shutdown Current	I_{SD}	$V_{EN}=0V$		5	12	μA
THRESHOLD VOLTAGE						
Input Over-Voltage Protection Threshold	V_{IN_OVP}			19		V
Input Over-Voltage Protection Hysteresis	$V_{IN_OVP_HY}$			2		V
EN High-Level Input Voltage	V_{ENH}		1.0	1.25	1.5	V
EN Low-Level Input Voltage	V_{ENL}		0.7	0.9	1.1	V
EN Pin Pull-Down Resistance	R_{EN_DN}	$V_{EN}=2V$		400		k Ω
Input Under-Voltage Lockout Threshold	V_{UVLO}		4.1	4.3	4.5	V
Input Under-Voltage Lockout Hysteresis	V_{UVLO_HY}			300		mV
SOFT START						
Turn On Delay Time	T_{ON_Delay}			0.3		ms
Soft Start Time	T_{SS}	V_{OUT} from 0 to 100%		1.2		ms
ON-TIME TIMER CONTROL						
Minimum On-Time	T_{ON_MIN}			50		ns
Minimum Off-Time	T_{OFF_MIN}			200		ns
MODULATOR CONTROL SECTION						
Regulated Feedback Voltage	V_{FB}		0.588	0.6	0.612	V
Switching Frequency	F_{SW}	CCM Mode	480	580	670	kHz
INTERNAL MOSFET						
High-Side Switch Resistance	$R_{DS(ON)_H}$	$I_{SW}=100mA$		80		m Ω
Low-Side Switch Resistance	$R_{DS(ON)_L}$	$I_{SW}=-100mA$		60		m Ω
OVER CURRENT LIMIT						
Low-side Switch Valley Current limit (Note)	I_{LIM_L}			3.8		A
PROTECTION SECTION						
Output Under-Voltage Protection Threshold	V_{UVP}	Hiccup Detect		66%		V_{FB}
Hiccup Power On-Time	T_{HICCUP_ON}			2		ms
Hiccup Power Off-Time	T_{HICCUP_OFF}			16		ms
Over Temperature Protection Threshold (Note)	OVP			165		$^{\circ}C$
Over Temperature Protection Hysteresis (Note)	OVP _{HY}			30		$^{\circ}C$

Note: Guaranteed by design.

■ OPERATION DESCRIPTION

Overview

The **UD18306** is a synchronous step-Down converter with input voltage range of 4.5V to 18V and output voltage as low as 0.6V. The **UD18306** adopts the COT architecture to achieve fast transient responses for high voltage step down applications. This device operates at 580kHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Input Under-Voltage Lockout

Input under-voltage lockout (UVLO) monitors the input voltage. When the input voltage is higher than the UVLO threshold voltage (typ.4.3V), the device turns on. Once the input voltage drops below the threshold with hysteresis (typ.0.3V), the device will shut down.

Input Over-Voltage Protection

Input over-voltage protection (OVP) monitors the input voltage. When the input voltage is above the OVP threshold voltage(typ.19V), the device shuts down. Once the input voltage drops below the threshold with hysteresis (typ.2V), the **UD18306** will return to normal operation automatically.

Soft Start

The **UD18306** has a built-in soft start circuit that can control the rate of output voltage rise, avoiding excessive surge currents during IC startup. The typical soft start time from 0% V_{OUT} to 100% V_{OUT} is usually 1.2ms.

EN Enable

The EN pin is provided to control the device turn-on and turn-off. When the EN pin voltage is above the V_{ENH} threshold (typ.1.25V), the device is enabled. When the EN pin voltage falls below the V_{ENL} threshold (typ.0.9V), the **UD18306** is disabled and enters shutdown mode.

Over Current Limit Protection and Output Short Protection

The **UD18306** has low-side MOSFET cycle- by-cycle current limit function, prevents the device from high load current condition. When inductor current valley value is larger than the valley current limit(typ.3.8A) during low side MOSFET on state, the device enters into valley over current protection mode and low side MOSFET keeps on state until inductor current drops down to the value equal or lower than the valley current limit, and then on time pulse could be generated and high side MOSFET could turn on again.

If the output is over current or output short to GND, the output voltage will drop. When the feedback voltage is below the output under voltage protection threshold(typ.66% V_{FB}), the **UD18306** enters into hiccup mode to periodically disable and restart switching operation. During hiccup mode, the IC will shut down for $T_{HICCUP\ OFF}$ (typ.16ms), and then attempt to recover automatically for $T_{HICCUP\ ON}$ (typ.2ms). The hiccup mode helps to reduce power dissipation and thermal rising during output short condition.

Output Under-Voltage Protection

The **UD18306** detects output under-voltage by monitoring the feedback voltage on the FB pin. When the feedback voltage is below 66% V_{FB} , the IC enters hiccup mode to periodically disable and restart the switch operation.

Over-Temperature Protection

The **UD18306** includes over-temperature Protection function. When the junction temperature exceeds about 165°C, the OTP will turn off the switch operation. Once the junction temperature drops to about 135°C, the IC will resume normal operation.

■ APPLICATION INFORMATION

Output Voltage Setting

Figure 1 shows the basic application circuit for the **UD18306**. The external resistance voltage divider can set the output voltage according to Equation (1).

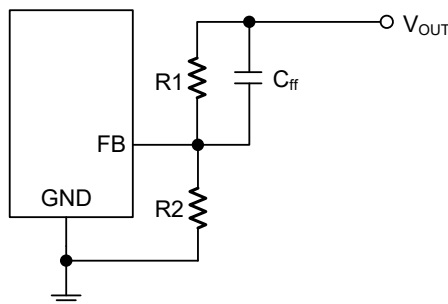


Figure. 1 Output Voltage Setting Circuits

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6 \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Current consumption and noise sensitivity need to be considered in the selection of resistance R2. A feed forward capacitor C_{ff} improves the loop bandwidth to make a fast transient response, but using a larger C_{ff} brings stability problems.

Inductor Selection

Inductance value, switching frequency, input voltage and output voltage together determine the ripple of inductance current and then affect the output ripple. The ripple of the inductor current can be obtained by Equation (2).

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times F_{SW}} \quad (2)$$

Where ΔI_L is the inductor current ripple, F_{SW} is the switching frequency.

To calculate the maximum inductor current under static load conditions, Equation (3) is given:

$$I_{L_MAX} = I_{OUT_MAX} + \frac{\Delta I_L}{2} \quad (3)$$

Recommended Components Selection

V_{OUT} (V)	R1 (k Ω)	R2 (k Ω)	C_{ff} (pF)	L (μ H)	C_{OUT} (μ F)
5.0	73.3	10	22	4.7	44 - 88
3.3	45.3	10	22	4.7	44 - 88
2.5	31.7	10	22	3.3	44 - 88
1.8	20	10	100	2.2	44 - 88
1.5	15	10	100	2.2	44 - 88
1.2	10	10	100	2.2	44 - 88
1.0	6.68	10	100	2.2	44 - 88

■ APPLICATION INFORMATION (Cont.)

Input Capacitor Selection

The input capacitor C_{IN} is needed to filter the fluctuations caused by the pulsating current at the drain of the high-side power MOSFET. Ceramic capacitors with X5R or a better grade ceramic capacitor dielectrics are highly recommended because of their low ESR and small temperature coefficients.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times F_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

A 22 μ F ceramic capacitor for most applications is sufficient. In applications, place the input capacitor C_{IN} as close as possible to the V_{IN} pin and GND pin of the IC. It is recommended to place the C_{IN} within 1cm of the IC.

Output Capacitor Selection

The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor's impedance. The output peak-to-peak ripple voltage ΔV_{OUT} , caused by the inductor current ripple, is composed of ESR ripple ΔV_{ESR} and capacitor ripple ΔV_{Cap} . The functional relationship of the output ripple is expressed by Equation 5:

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{Cap} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{8 \times C_{OUT} \times F_{SW}} \quad (5)$$

Where R_{ESR} is equivalent impedance on capacitor.

Two 22 μ F ceramic can satisfy most applications.

When output Capacitor is only Electrolytic capacitors there is no need to add a C_{ff} (feed forward capacitor).

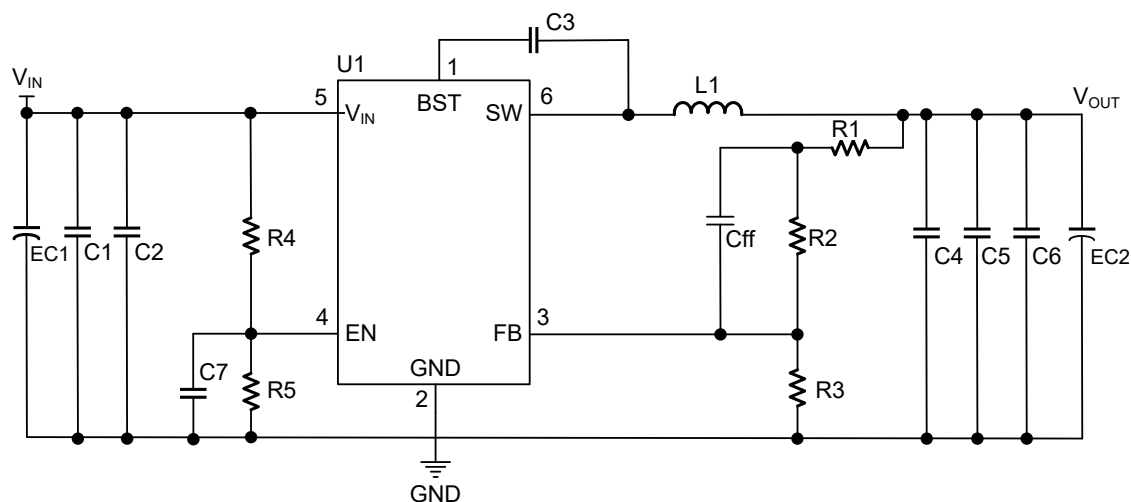
Boost Capacitor Selecting

The boost capacitor (C_{BST}) between BST pin and SW pin is used to create a voltage rail above V_{IN} . For most applications, it is recommended to use ceramic capacitors with X5R specifications, capacitance of 0.1 μ F, and 0603 packaging. The rated voltage of the capacitor should be 6.3V or higher.

Layout Consideration

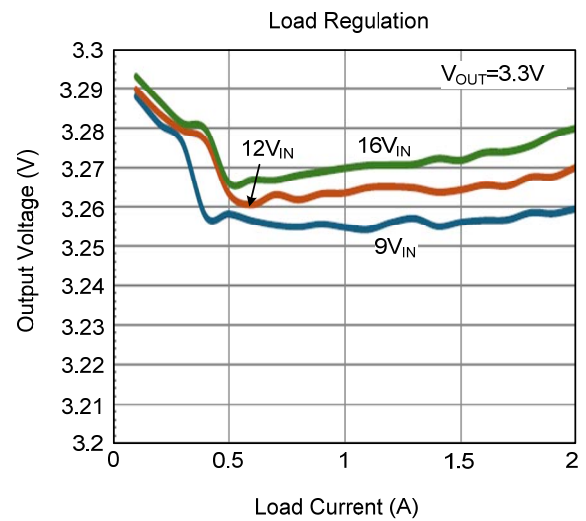
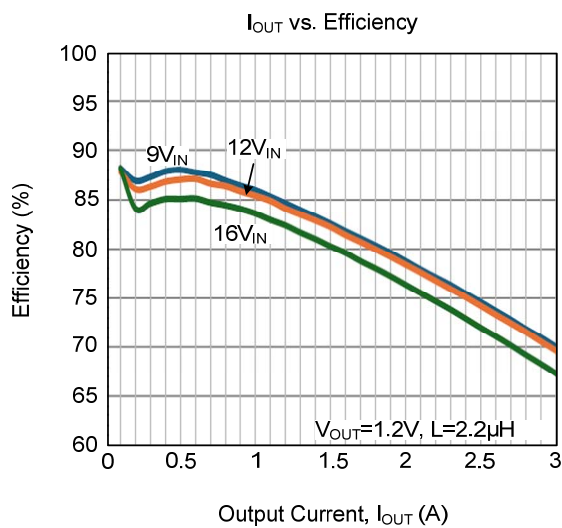
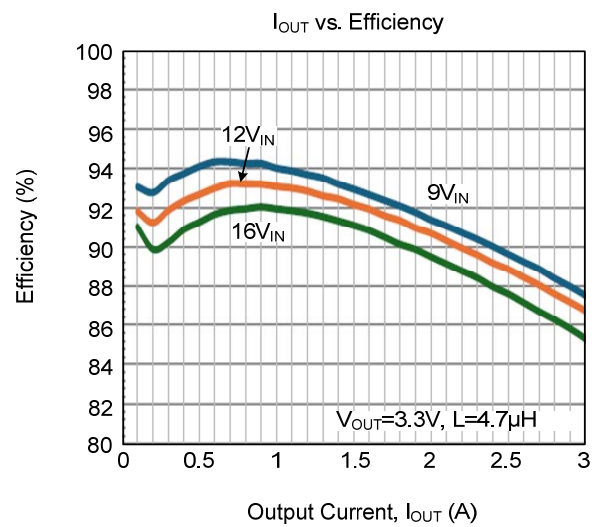
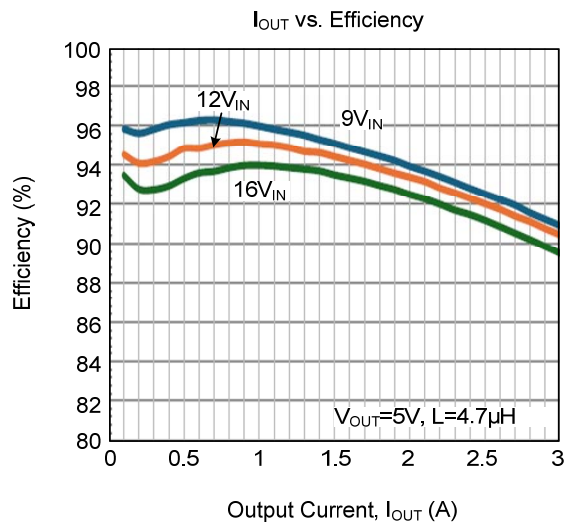
1. V_{IN} and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. Place the input capacitor close to the V_{IN} and GND pins.
3. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
4. A separate V_{OUT} path should be connected to the upper feedback resistor.
5. Voltage feedback loop should be placed away from the high-voltage switching trace.
6. The trace of the V_{FB} node should be as small as possible to avoid noise coupling.
7. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

■ TYPICAL APPLICATION CIRCUIT



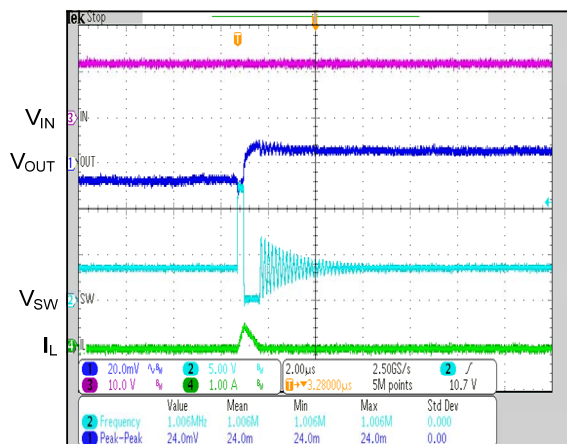
Qty.	Designator	Value	
1	C1	22 μ F	
2	C2, C3	0.1 μ F	
2	C4, C5	22 μ F	
1	C _{ff}	V _{OUT} =5, 3.3V	22pF
		V _{OUT} =1V	100pF
0	C6, C7	NC	
0	EC1, EC2	NC	
1	R1	0 Ω	
1	R2	V _{OUT} =5V	73.3k Ω
		V _{OUT} =3.3V	45.3k Ω
		V _{OUT} =1V	6.68k Ω
1	R3	10k Ω	
1	R4	100k Ω	
0	R5	NC	
1	L1	V _{OUT} =5V, 3.3V	4.7 μ H
		V _{OUT} =1V	2.2 μ H
1	U1	/	

TYPICAL CHARACTERISTICS

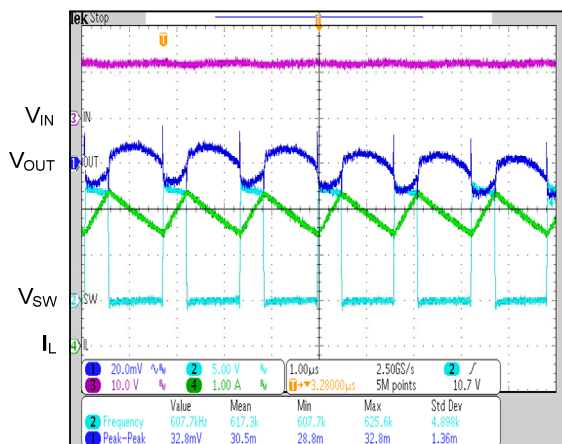


TYPICAL CHARACTERISTICS (Cont.)

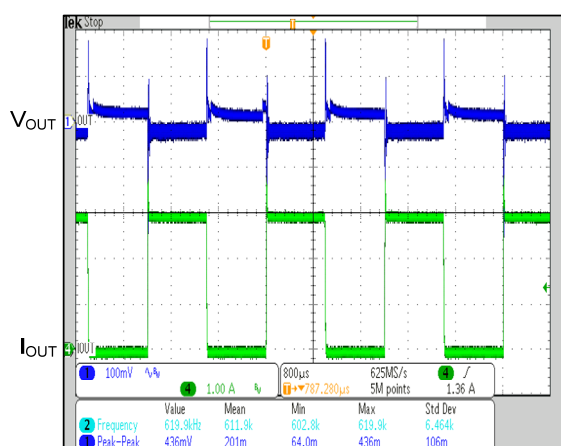
Steady State Operation
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0A$)



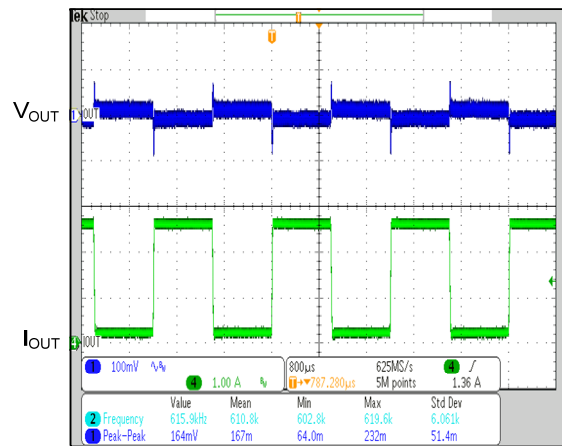
Steady State Operation
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=3A$)



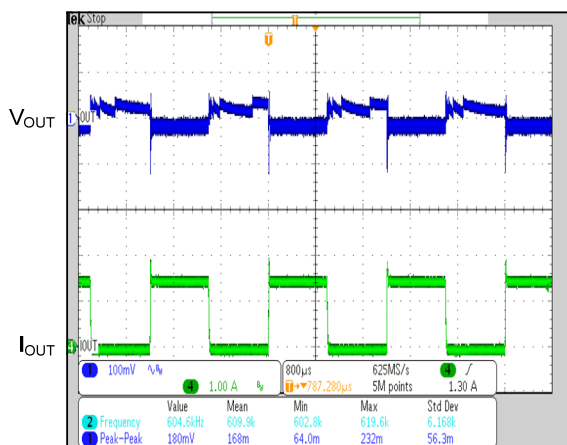
Load Transient
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0A$ to $3A$)



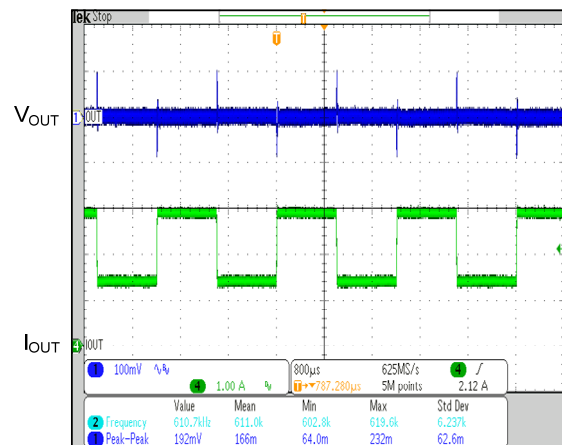
Load Transient
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0A$ to $2.7A$)



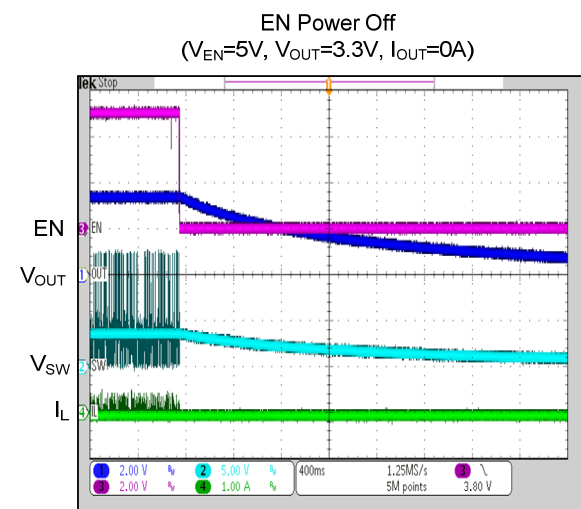
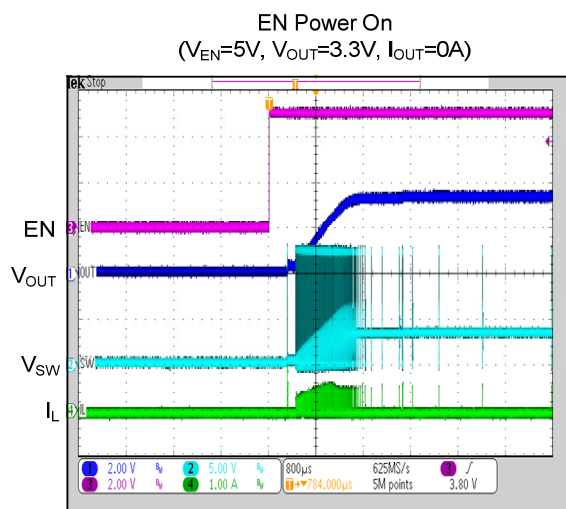
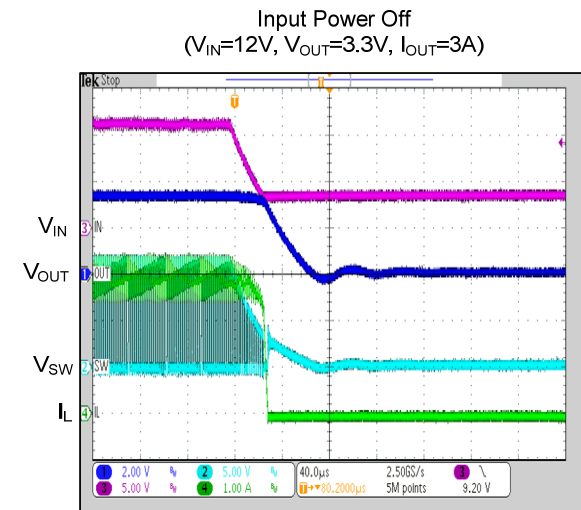
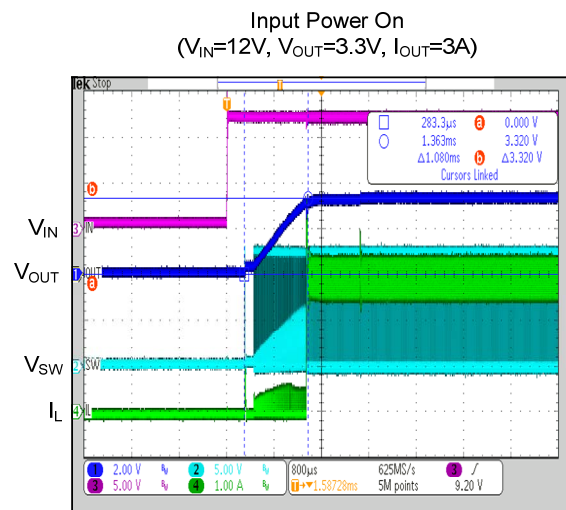
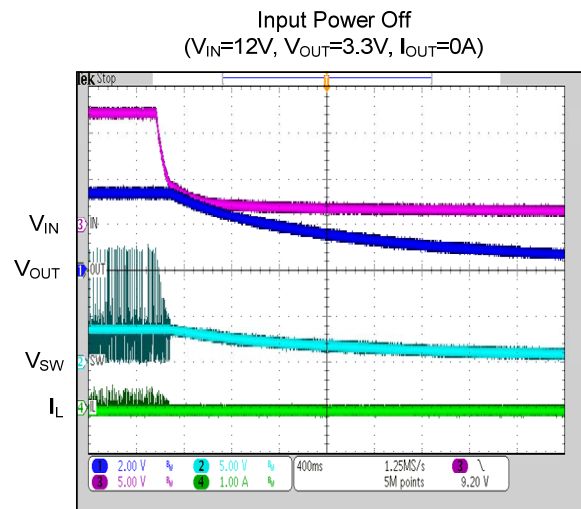
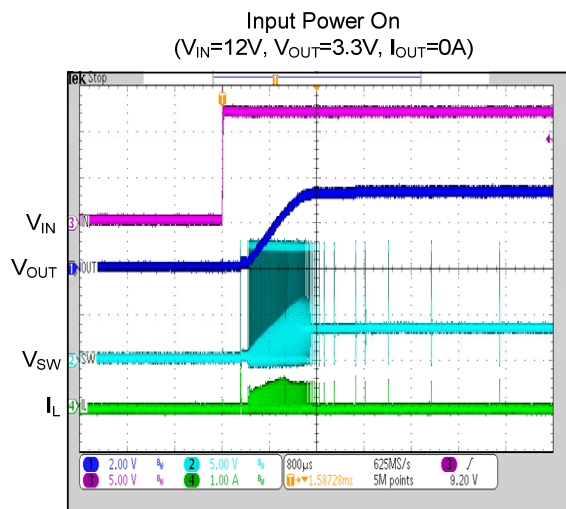
Load Transient
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0A$ to $1.5A$)



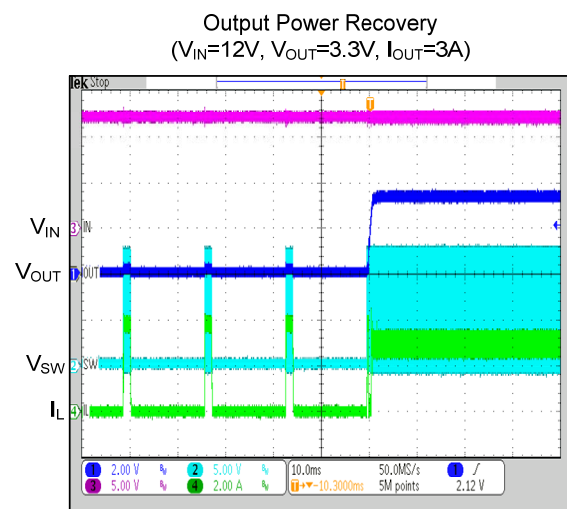
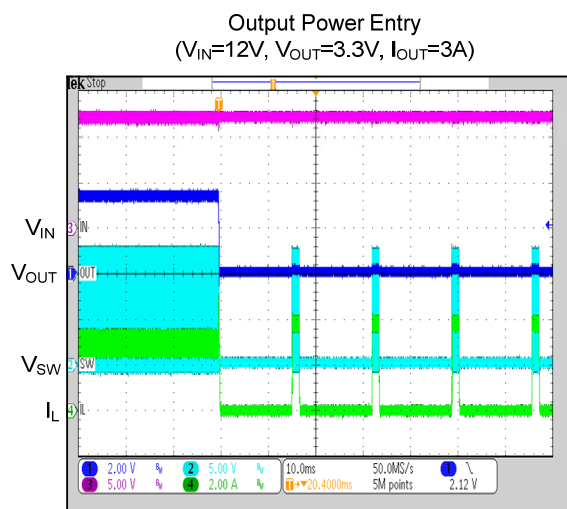
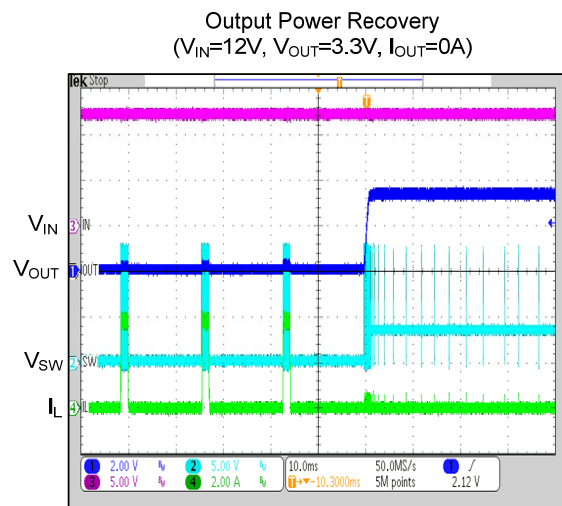
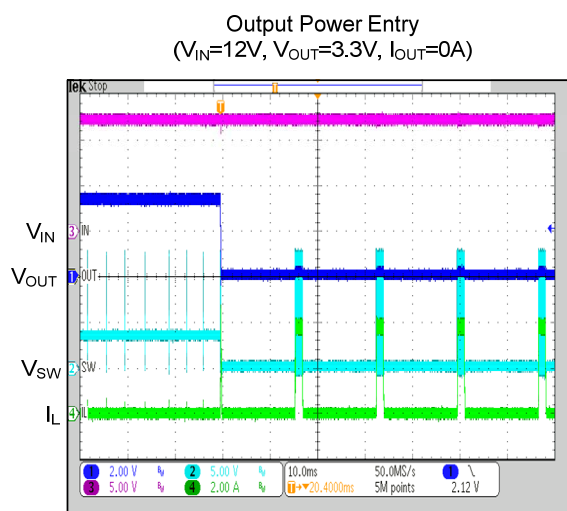
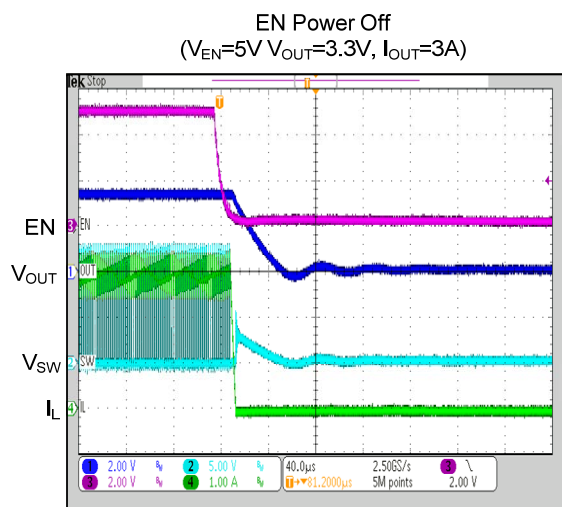
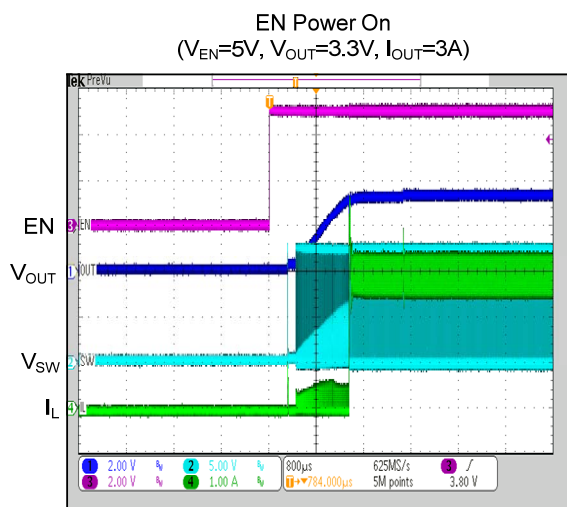
Load Transient
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=1.5A$ to $3A$)



TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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