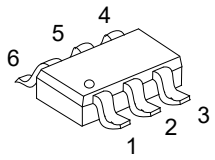
36V, 2A, 520kHz SYNCHRONOUS STEP-DOWN CONVERTER



SOT-26

■ DESCRIPTION

The UTC **UD36202** is an easy to use synchronous step-down Buck. Which integrated low on resistance high-side and low-side power MOSFETs. The UTC **UD36202** can deliver 2A of output current efficiently with constant on time (COT) control for fast loop response. The UTC **UD36202** achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses. The UTC **UD36202** has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open short protection and thermal shutdown in case of excessive power dissipation.

■ FEATURES

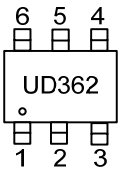
* 4.5V to 36V Wide Input Range
* 2A Continuous Output Current
* 135mΩ/85mΩ Internal Power MOSFETs
* Constant On Time Control for Fast Loop Response
* 520kHz Switching Frequency
* Pulse Frequency Modulation at Light Load
* Support Up to 98% Large Range Duty Cycle
* Internal Soft Start
* Output Voltage Adjustable from 0.596V
* Support Pre-Biased Output Startup
* Full Protection, Over Current Protection and Hiccup, Output Over Voltage Protection, FB Open Short Protection, Over Temperature Protection

■ ORDERING INFORMATION

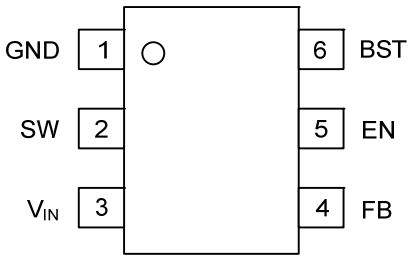
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UD36202L-AG6-R	UD36202G-AG6-R	SOT-26	Tape Reel

UD36202G-AG6-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AG6: SOT-26 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



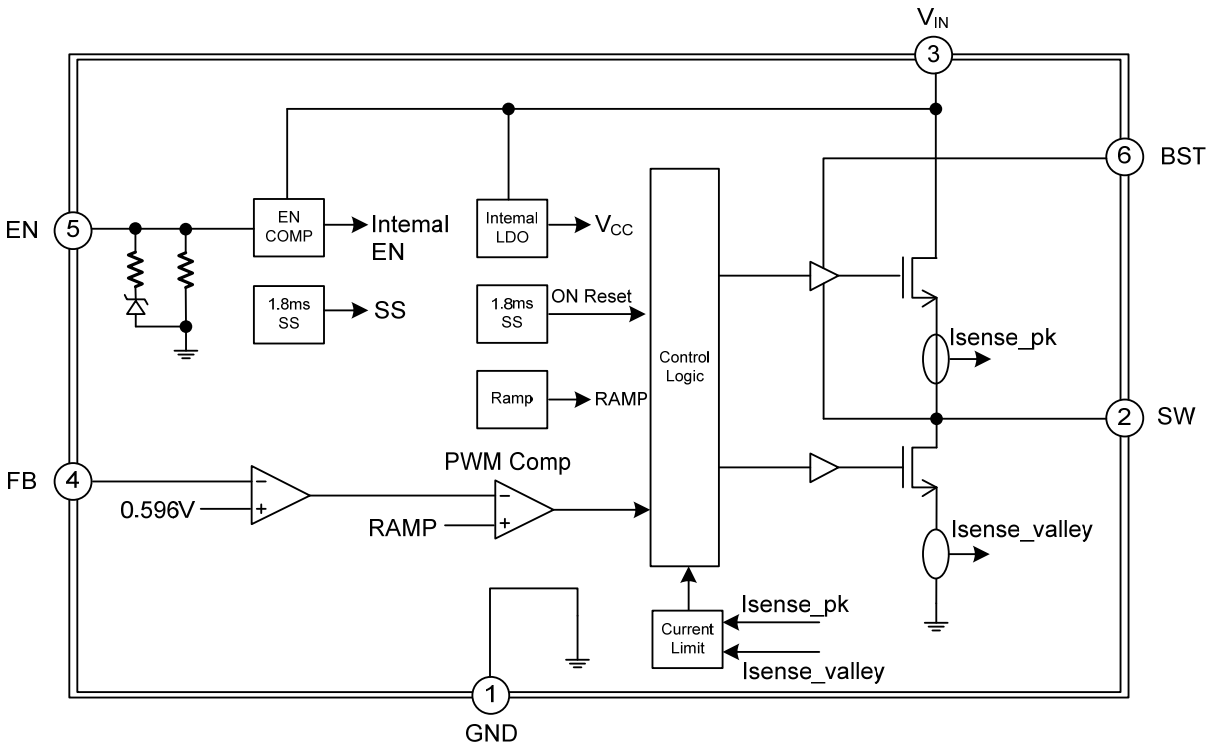
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	PIN	DESCRIPTION
1	GND	P	Power Ground terminal.
2	SW	O	Switching output of the convertor. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.
3	V_{IN}	P	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors C_{IN}. Input bypass capacitors must be directly connected to this pin and GND.
4	FB	I	Feedback input to the convertor. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
5	EN	I	Precision enable input to the convertor. Do not float. High = on, Low = off. Can be tied to V_{IN} by a resistor. Precision enable input allows adjustable UVLO by external resistor divider.
6	BST	O	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to GND	V_{IN}	-0.3~38	V
SW to GND	SW	-0.7 (-5V in 10ns) ~ V_{IN} + 0.7	V
Max. Input Current to EN Pin	EN	100 (Note 2)	μA
BST to SW Voltage		-0.3 ~ 6	V
All Other Pins		-0.3 ~ 6	V
Operating Junction Temperature	T_J	-40 ~ +150	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. For details on ENs ABS max rating, please refer to the Enable Control section.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
BST to SW	BST	4 ~ 5	V
FB to GND	FB	0 ~ 1	V
EN to GND	EN	0 ~ 5	V
V_{IN} to GND	V_{IN}	4.5 ~ 36	V
V_{OUT} to GND	V_{OUT}	0.6 ~ V_{IN}×D_{MAX}(Note) or 13V	V
Max Continuous Output Current	I_{OUT}	2	A

Note: D_{MAX} = T_{ON_MAX} / (T_{ON_MAX} + T_{OFF_MIN}). Typical value is 98%.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	100	°C/W

■ ELECTRICAL CHARACTERISTICS (V_{IN}=12V, V_{OUT}=2V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} UVLO Rising Threshold	V_{IN_UVR}		4.1	4.25	4.4	V
V_{IN} UVLO Falling Threshold	V_{IN_UVF}		3.85	4.0	4.15	V
V_{IN} UVLO Hysteresis	$V_{IN\_UV\_hys}$			0.25		V
Shutdown Supply Current	I_{QS}	V_{EN} < 0.3V V_{IN}=12V		1	3	μA
Quiescent Supply Current	I_Q	No load, V_{FB} =0.83V, No switching		160		μA
High-Side Leakage	L_{KG_HS}	V_{EN} = 0V, V_{SW} = 0V			1	μA
Low-Side Leakage	L_{KG_LS}	V_{EN} = 0V, V_{SW} = 12V			1	μA
Feedback Voltage	V_{FB}	T_A=25°C	584	596	608	mV
		T_A=-40°C ~ +125°C	581	596	611	mV
Hiccup Threshold	FB_{UVP}			280		mV
Feedback Leakage	I_{LK_FB}	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
High-Side Switch on Resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		135		mΩ
Low-Side Switch on Resistance	R_{ON_LS}	V_{IN} = 12V		85		mΩ
Low-Side Current limit	I_{LIM_LS}	T_A=-40°C ~ +125°C	2.3	2.9	3.5	A
High-Side Current limit	I_{LIM_HS}	T_A=-40°C ~ +125°C	3.6	5.3		A
Zero Crossing	I_{LIM_ZCD}			100		mA
Soft-Start time	T_{SS}	V_{FB} from 0% to 100%		1.8		ms
Oscillator Frequency	F_{SW}		440	520	600	kHz
Minimum Switch ON Time (Note)	T_{ON_MIN}			80		ns
Minimum Switch OFF Time (Note)	T_{OFF_MIN}			120		ns
Max. Duty Cycle	D_{MAX}			98%		%
Enable Rising Threshold	V_{EN_R}	Low to high	1.1	1.2	1.3	V
Enable Falling Threshold	V_{EN_F}	High to low	0.8	0.9	1.0	V
Enable Threshold Hysteresis	V_{EN_Hys}			0.2		V
Enable Input Resistor.	R_{EN}			1500		kΩ
Thermal Shutdown (Note)	T_{OTP_R}			150		°C
OTP hysteresis (Note)	T_{OTP_Hys}			20		°C

Note: Guaranteed by design.

■ FUNCTION DESCRIPTIONS

Pulse-Width Modulation (PWM) Control

The **UD36202** is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. To avoid shoot- through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

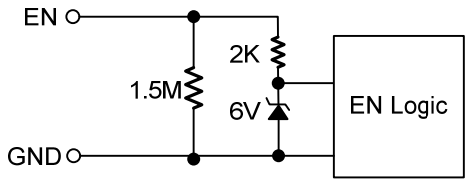
With the load decrease, the inductor current decrease too. Once the inductor current touch zero, the operation is transition from continuous-conduction-mode (CCM) to discontinuous- conduction-mode (DCM).

When the **UD36202** works in pulse-frequency modulation (PFM) mode during light-load operation, the UD36202 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side will be off. The output capacitors discharge slowly to GND through R1 and R2. When V_{FB} drops below the reference voltage, the HS-FET is turned on again. This operation improves device efficiency greatly when the output current is low.

Enable (EN) Control

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1.5MΩ resistor from EN to GND allows EN to be floated to shut down the chip. EN is clamped internally using a 6V Zener diode. EN can connected to V_{IN} directly by a resistor.

The EN Pin can connect to V_{IN} by a pull-up resistor, but EN input current need below 100μA. For example, if V_{IN}=24V, the I_{Zener}=(24-6)/$R_{PULL-UP}$ < 100μA, So, $R_{PULL-UP}$ > 180KΩ.



Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The **UD36202** UVLO comparator monitors the input voltage. The UVLO rising threshold is about 4.25V, while its falling threshold is consistently 4V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1V. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 1.8ms internally.

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The **UD36202** has a valley current-limit control. During LS-FET on, the inductor current is monitored. If the current is higher than valley current limit, the high side will not turn on again. The output voltage drops until V_{FB} is below the under voltage (UV) threshold (typically 280mV). Once UV is triggered, the **UD36202** enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

■ FUNCTION DESCRIPTIONS (Cont.)

Pre-Bias Start-Up

The **UD36202** is designed for monotonic start-up into pre-biased loads. If the output is pre- biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

Output Over-Voltage Protection

The **UD36202** has implement output over-voltage protection. If output voltage rises above the regulated voltage, IC will stop switching to avoid the output voltage overshoot.

Input Over-Voltage Protection

The **UD36202** has implement the input over voltage protection. IC will stop switching if input voltage rises above 39V. This will increase the IC robustness against the surge voltage on the input. In the input over-voltage condition when input voltage drops below 38V, IC will restart switching again and output voltage will back to the regulated value after soft start.

Large Duty Cycle Operation

When **UD36202** will automatically extend the frequency to support the application when V_{IN} is close to V_{OUT}. The frequency extend circuit will be triggered when T_{OFF_MIN} time is reached. The **UD36202** can support up to 98% maximum duty cycle.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

■ APPLICATION INFORMATION

The **UD36202** output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.596V. The feedback network is shown below Figure.

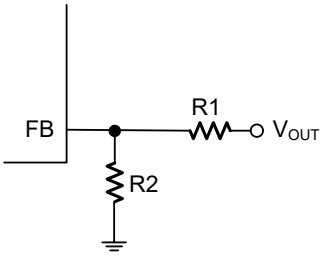


Figure 1. Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT}=V_{FB}\times\frac{R1+R2}{R2} \quad (1)$$

Selecting the Inductor

For most applications, use a 3.3μH to 47μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a small DC resistance.

For most designs, the inductance value can be derived from Equation:

$$L=\frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times\Delta I_L\times f_{SW}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{L\_MAX}=I_{LOAD}+\frac{\Delta I_L}{2} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (μF)
5	110	15	10	22
3.3	68	15	10	22

Note: For a detailed design circuit, please refer to the Typical Application Circuits.

Selecting the Output Capacitor

The output capacitor (C2, C3) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

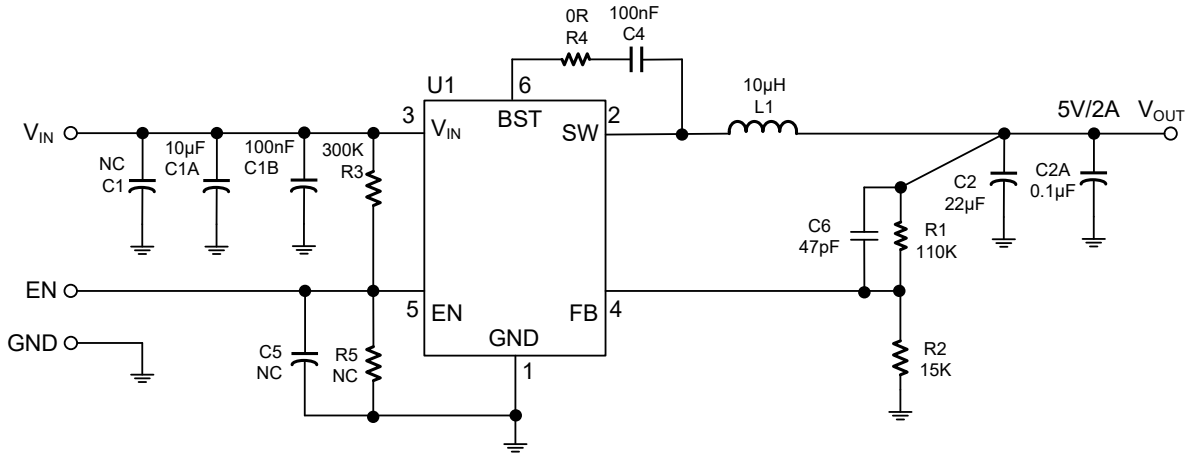
$$\Delta V_{OUT}=\frac{V_{OUT}}{f_{SW}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_{SW}\times C_{OUT}}\right) \quad (4)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also affect the stability of the regulation system. The **UD36202** can be optimized for a wide range of capacitance and ESR values

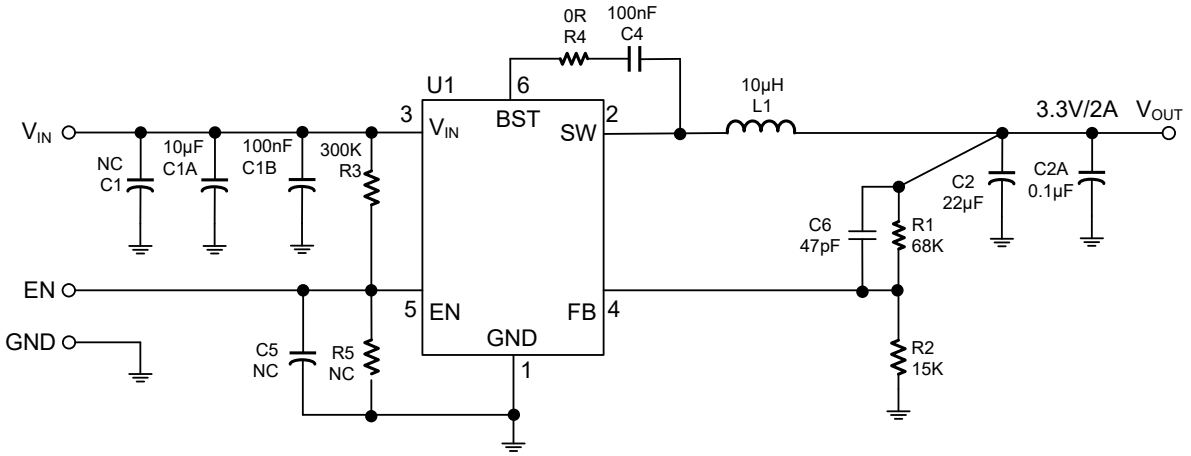
■ TYPICAL APPLICATION CIRCUIT

V_{IN}=12V, V_{OUT}=5V/2A



Note: C6 is optional for better transient performance.

V_{IN}=12V, V_{OUT}=3.3V/2A



Note: C6 is optional for better transient performance.