



UPGE85N33

Insulated Gate Bipolar Transistor

WITH ANTI-PARAALLEL DIODE FOR PDP SUSTAIN CIRCUIT

■ DESCRIPTION

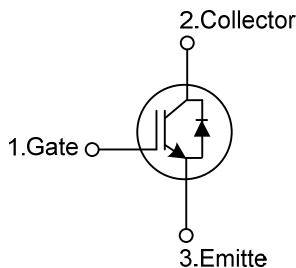
The UTC **UPGE85N33** is with Anti-Parallel Diode for PDP Sustain Circuit. it uses UTC's advanced technology to provide customers with high input impedance, high switching speed and low conduction loss, etc.

The UTC **UPGE85N33** is suitable for high voltage switching, high frequency switch mode power supplies.

■ FEATURES

- * $V_{CE(SAT)} \leq 1.9\text{ V @ } I_C=50\text{A, } V_{GE}=15\text{V}$
- * $V_{CE(SAT)} \leq 2.9\text{ V @ } I_C=100\text{A, } V_{GE}=15\text{V}$
- * High switching speed
- * High input impedance
- * Low conduction loss

■ SYMBOL

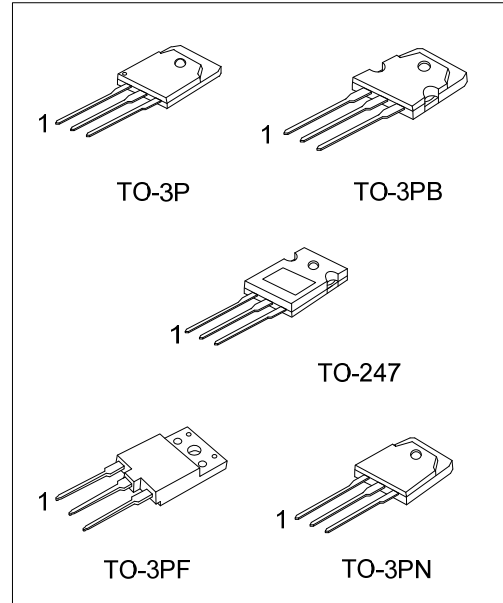


■ ORDERING INFORMATION

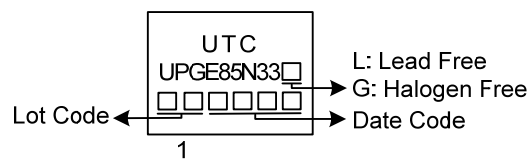
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UPGE85N33L-T3B-T	UPGE85N33G-T3B-T	TO-3PB	G	C	E	Tube
UPGE85N33L-T3F-T	UPGE85N33G-T3F-T	TO-3PF	G	C	E	Tube
UPGE85N33L-T3N-T	UPGE85N33G-T3N-T	TO-3PN	G	C	E	Tube
UPGE85N33L-T3P-T	UPGE85N33G-T3P-T	TO-3P	G	C	E	Tube
UPGE85N33L-T47-T	UPGE85N33G-T47-T	TO-247	G	C	E	Tube

Note: Pin Assignment: G: Gate C: Collector E: Emitter

UPGE85N33G-T3P-T	(1)Packing Type	(1) T: Tube
	(2)Package Type	(2) T3B: TO-3PB, T3F: TO-3PF, T3P: TO-3P, T3N: TO-3PN, T47: TO-247
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage		V _{CES}	330	V
Gate to Emitter Voltage Continuous		V _{GES}	±30	V
Continuous Collector Current	T _C =25°C	I _C	170	A
	T _C =100°C		85	A
Collector Current Pulsed (Note 2)		I _{CM}	240	A
Continuous Forward Current	T _C =25°C	I _F	85	A
	T _C =100°C		42.5	A
Forward Current Pulsed		I _{FM}	90	A
Peak Diode Recovery dv/dt (Note 3)		dv/dt	5.7	V/ns
Power Dissipation	TO-247	P _D	260	W
	TO-3P		265	W
	TO-3PB			
	TO-3PN		130	W
	TO-3PF			
Junction Temperature		T _J	-55 ~ +150	°C
Storage Temperature Range		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. I_F ≤ 30A, di/dt ≤ 200A/μs, V_{CC} ≤ BV_{CES}, Starting T_J = 25°C.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Case	TO-247	θ _{JC}	0.59	°C/W
	TO-3P		0.47	°C/W
	TO-3PB			
	TO-3PN		0.96	°C/W
	TO-3PF			

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage	BV _{CES}	I _C =250μA, V _{GE} =0V	330			V
Collector-Emitter Leakage Current	I _{CES}	V _{CE} =330V, V _{GE} =0V			10	μA
Gate to Emitter Leakage Current	I _{GES}	V _{CE} =0V, V _{GE} =±20V			±100	nA
ON CHARACTERISTICS						
Collector-Emitter Saturation Voltage	V _{CE(SAT)}	I _C =50A, V _{GE} =15V	T _J =25°C		1.9	V
			T _J =150°C		1.8	V
		I _C =100A, V _{GE} =15V	T _J =25°C		2.9	V
			T _J =150°C		2.6	V
Gate to Emitter Threshold Voltage	V _{GE(TH)}	I _C =250μA, V _{CE} =V _{GE}	3.5		6.0	V
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{IES}	V _{CE} =25V, V _{GE} =0V, f=1MHz		3270		pF
Output Capacitance	C _{OES}			300		pF
Reverse Transfer Capacitance	C _{RES}			31		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q _G	I _C =85A, V _{CE} =280V, V _{GE} =10V		89		nC
Gate-Emitter Charge	Q _{GE}			25		nC
Gate-Collector Charge	Q _{GC}			36		nC
Current Turn-On Delay Time	t _{D(ON)}	I _C =85A, V _{CE} =15V, V _{CE} =240V, R _G =25Ω		47		ns
Current Rise Time	t _R			100		ns
Current Turn-Off Delay Time	t _{D(OFF)}			270		ns
Current Fall Time	t _F			525		ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Voltage Drop	V _{FM}	I _F =85A, V _{GE} =0V			2.5	V
Reverse Recovery Time	t _{rr}	I _F =85A, dI/dt=100A/μS, V _{CE} =240V		16.4		ns
Reverse Recovery Charge	Q _{rr}			411		nC

Note: Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

■ TEST CIRCUIT AND WAVEFORMS

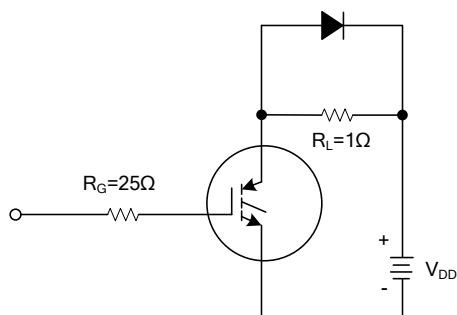


Fig 1. INDUCTIVE SWITCHING TEST CIRCUIT

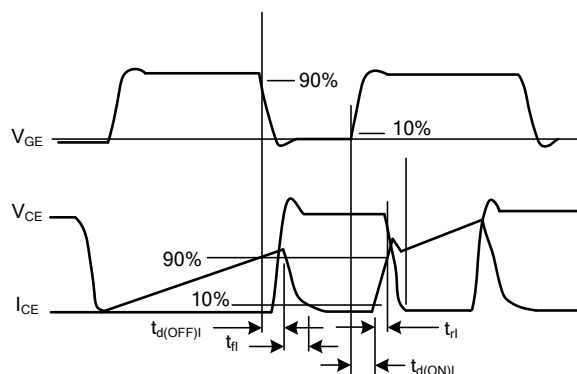


Fig 2. SWITCHING TEST WAVEFORMS

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