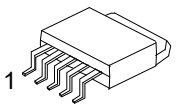
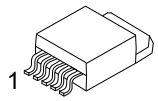
UR6515A

CMOS IC

3A DDR BUS TERMINATION REGULATOR



TO-263-5



TO-252-5

■ DESCRIPTION

The **UR6515A** is a linear regulator providing up to 3A transient peak current sourcing and sinking capability for DDR SDRAM bus terminator applications while regulating an output voltage to within 40mV. It contains a high speed operational amplifier which provides fast load transient response and only requires 10uF of ceramic output capacitance.

The **UR6515A** output termination voltage tracks the reference voltage applied at V_{REF} pin. A resistor divider connected to V_{IN}, GND and V_{REF} pins is used to force the reference voltage to V_{REF} pin. Additional features include current limiting protection and thermal shutdown protection.

■ FEATURES

* DDR1/ DDR2 termination voltage applications
* Low output voltage offset within 20mV
* Source and sink 3A peak current
* Adjustable output voltage by external resistors
* Integrated power MOS devices
* Suspend to RAM(STR) functionality
* Current Limiting Protection
* Thermal Shutdown Protection
* Cost-effective and easy to use

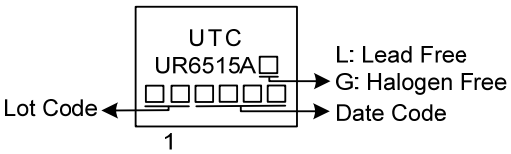
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UR6515AL-TN5-R	UR6515AG-TN5-R	TO-252-5	Tape Reel
UR6515AL-TQ5-R	UR6515AG-TQ5-R	TO-263-5	Tape Reel
UR6515AL-TQ5-T	UR6515AG-TQ5-T	TO-263-5	Tube

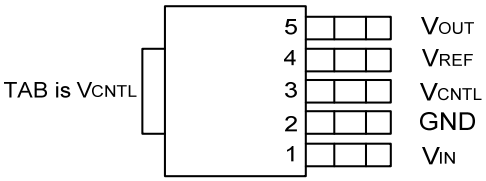
UR6515AG-TN5-R
- (1)Packing Type
- (2)Packing Type
- (3)Green Package

(1) R: Tape Reel, T:Tube
(2) TN5: TO-252-5, TQ5: TO-263-5
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



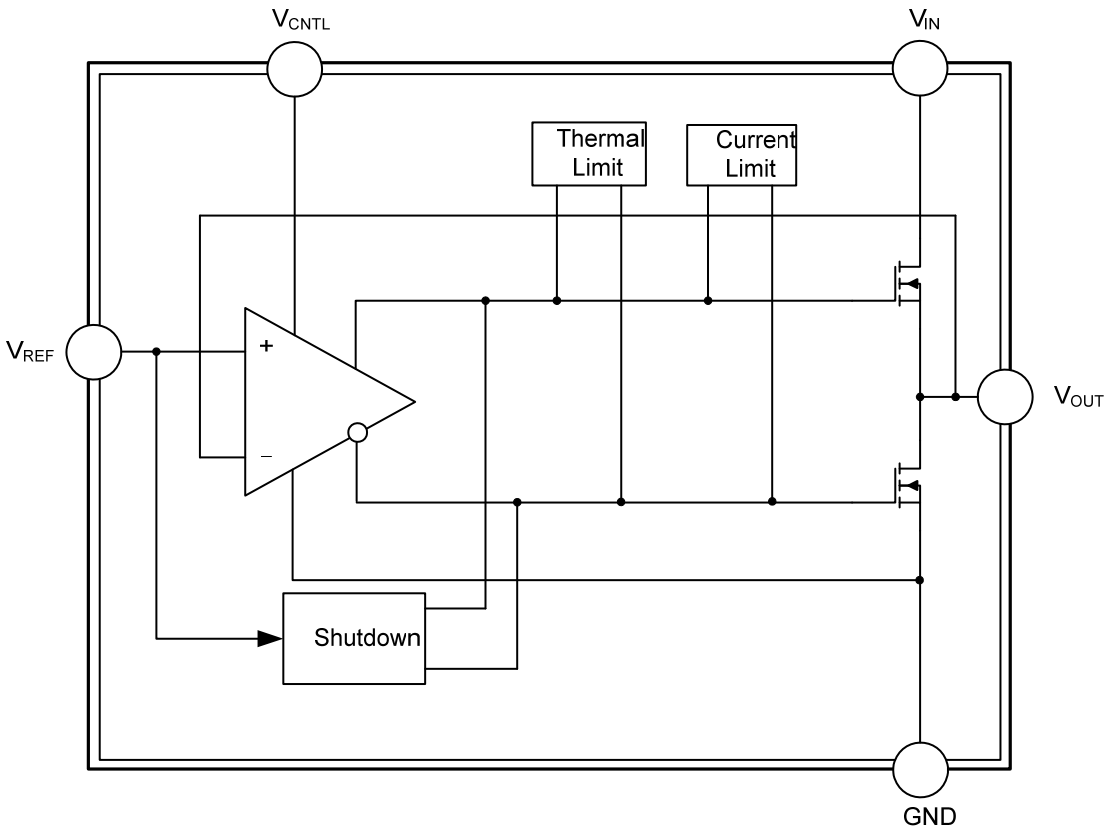
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

PIN NAME	PIN TYPE	PIN DESCRIPTION
V_{IN}	I	Power supply pin for the VOUT output
GND	O	Ground pin
V_{CNTL}	I	Power supply pin for the internal control circuits
V_{REF}	I	Reference voltage input and active-low shutdown control pin
V_{OUT}	O	Output voltage pin

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
V_{CNTL} Control Voltage		V_{CNTL}	7	V
V_{IN} Supply Voltage		V_{IN}	7	V
Power Dissipation (T_A=25°C)	TO-252-5	P_D	1.471	W
	TO-263-5		1.923	W
Junction Temperature		T_J	+125	°C
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 1)	TO-252-5	θ_{JA}	68	°C/W
	TO-263-5		52	°C/W
Junction to Case	TO-252-5	θ_{JC}	8	°C/W
	TO-263-5		7.7	°C/W

Note: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

■ RECOMMENDED OPERATING CONDITIONS (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{CNTL} Control Voltage	V_{CNTL}	5 or 3 ± 5%	V
V_{IN} Supply Voltage	V_{IN}	2.5 ~ 1.5 ± 3%	V
V_{REF} Input Voltage	V_{REF}	1.25 ~ 0.75 ± 3%	V
Junction Temperature	T_J	-40 ~ +125	°C

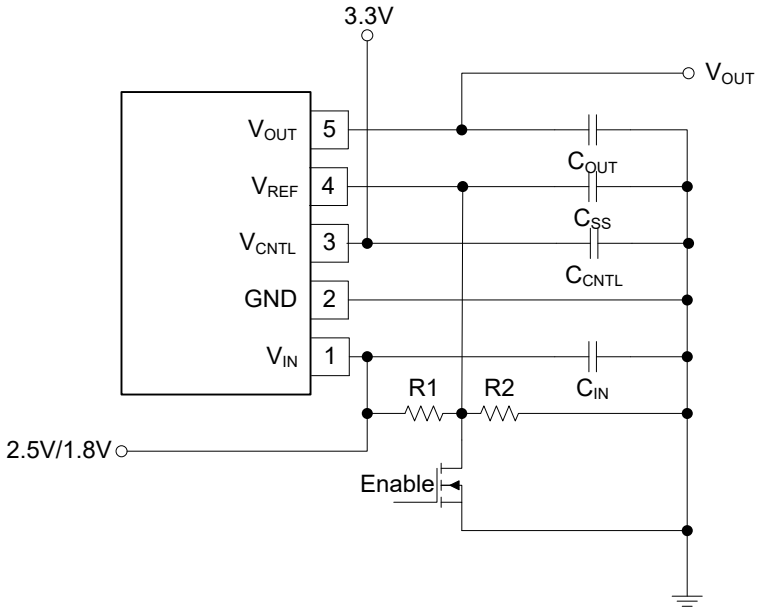
Notes: 1. All voltage values are with respect to the network ground terminal unless otherwise noted.
2. The V_{OUT} tracks the VREF with additional voltage offset and load regulation.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

(V_{IN}=2.5V/1.8V, V_{CNTL}=3.3V, V_{REF}=1.25V/0.9V, C_{OUT} = 10μF (Ceramic))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
Operation Current of V_{CNTL}	I_{CNTL}	I_{OUT} =0A		1	2.5	mA
Standby Current	I_{STB}	V_{REF}<0.2V, R_{LOAD}=180Ω		50	90	μA
OUTPUT VOLTAGE (DDR/DDR II/DDR III)						
Output Voltage Offset (V_{REF}-V_{OUT})	V_{OS}	I_{OUT} =0A	-20		20	mV
Load Regulation(DDR1/2)	ΔV_{LOAD}	I_{OUT} =±1.5A		0.8/1.2	2/3	%
PROTECTION						
Current Limit	I_{LIMIT}	V_{IN}=2.5V/1.8V	3			A
Thermal Shutdown Temperature	T_{SD}	V_{CNTL}=3.3V~5V	125	150		°C
Thermal Shutdown Hysteresis	ΔT_{SD}	V_{CNTL}=3.3V~5V		50		°C
V_{REF} Shutdown						
Shutdown Threshold	V_{IH}	Enable	0.8			V
	V_{IL}	Shutdown			0.2	V

■ TYPICAL APPLICATIONS CIRCUITS

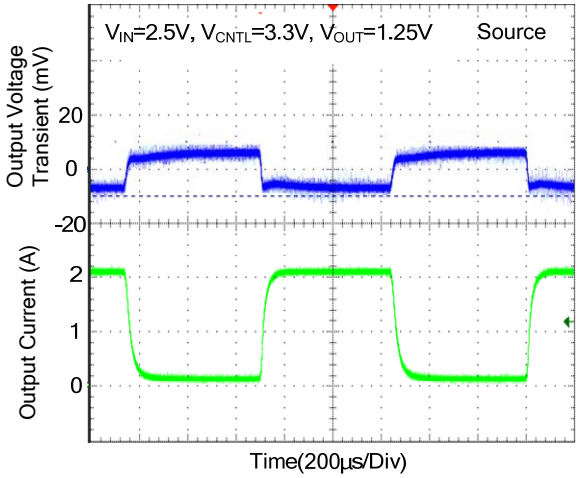


Notes: 1. R1=R2=100KΩ, C_{OUT}=10μF(Ceramic)+1000μF under the worst case testing condition
C_{SS}=1μF, C_{IN}=470μF(Low ESR), C_{CNT}L=47μF

2. $V_{REF} = \frac{R_2}{R_1 + R_2} V_{IN}(V)$, V_{OUT} track V_{REF}

■ TYPICAL CHARACTERISTICS

1.25 V_{TT}@2A Transient Response



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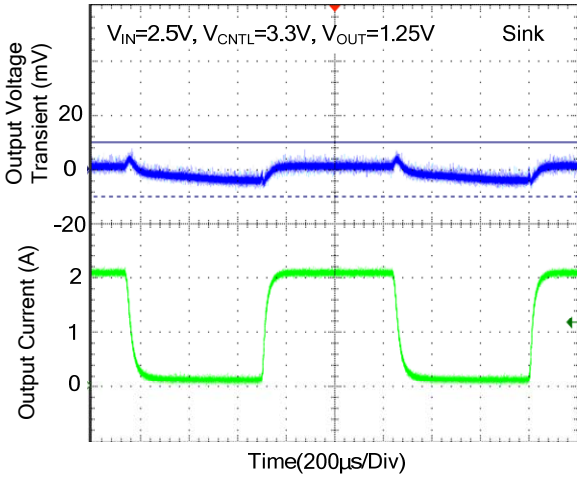
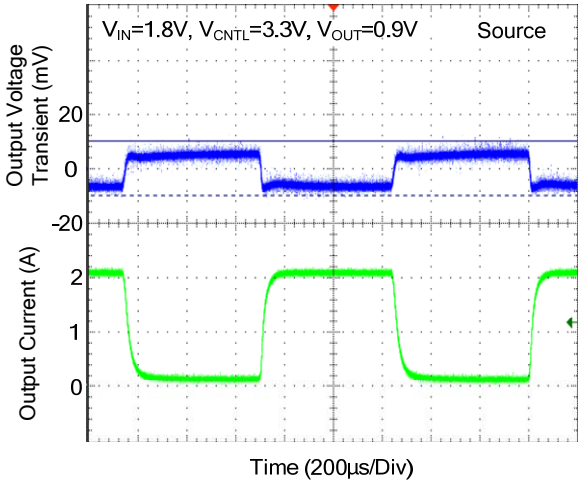


0.9 V_{TT}@2A Transient Response



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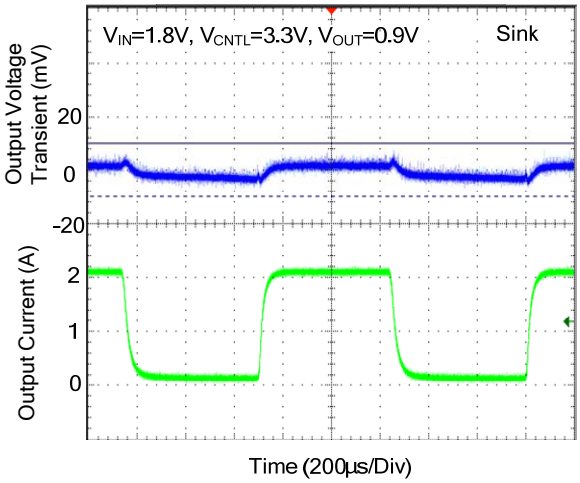
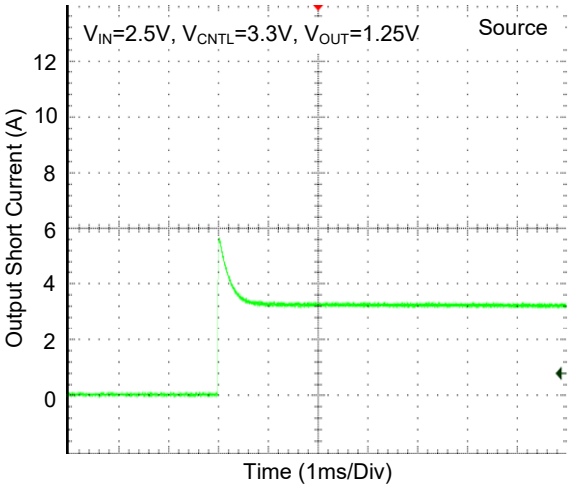


■ TYPICAL CHARACTERISTICS (Cont.)

Output Short Circuit Protection



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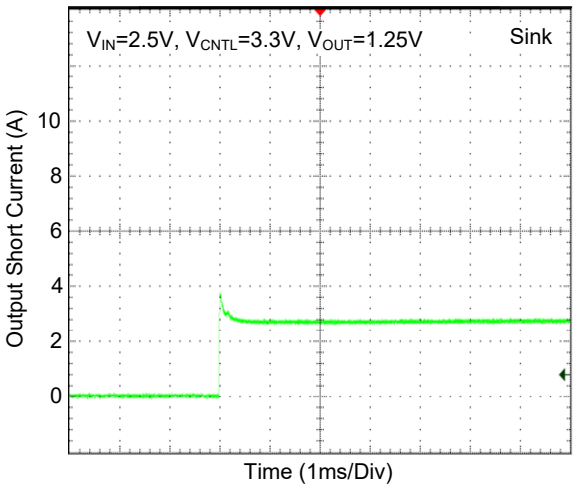

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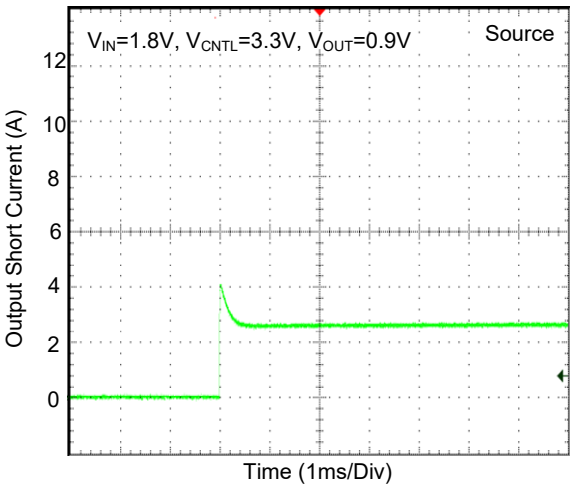

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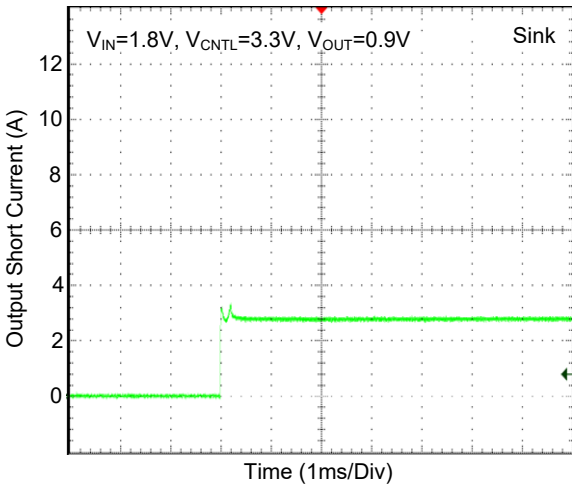
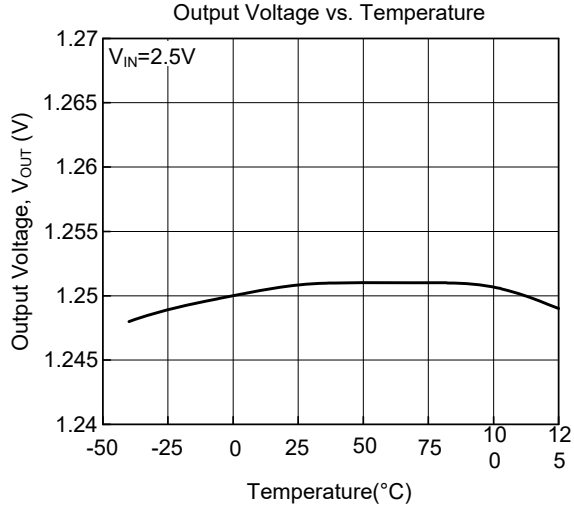


Output Voltage vs. Temperature



Output Voltage vs. Temperature