

**USG10R088M****POWER MOSFET**

**N-CHANNEL SGT  
ENHANCEMENT POWER  
MOSFET**

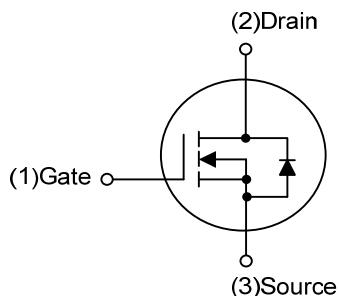
■ **DESCRIPTION**

The UTC **USG10R088M** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low  $R_{DS(ON)}$  characteristic by high cell density trench technology.

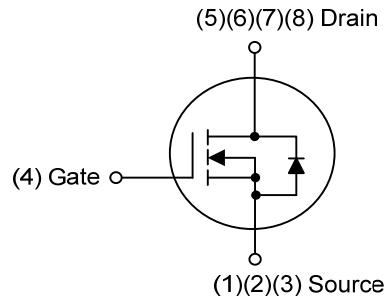
■ **FEATURES**

- \*  $R_{DS(ON)} \leq 8.8 \text{ m}\Omega @ V_{GS}=10V, I_D=32A$
- \*  $R_{DS(ON)} \leq 11 \text{ m}\Omega @ V_{GS}=4.5V, I_D=20A$
- \* Extremely low on-resistance  $R_{DS(ON)}$
- \* Excellent Low Ciss

■ **SYMBOL**



TO-252 / TO-220F1



PDFN5x6

■ **ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
USG10R088ML-TF1-T	USG10R088MG-TF1-T	TO-220F1	G	D	S	-	-	-	-	-	Tube
USG10R088ML-TN3-R	USG10R088MG-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
USG10R088ML-P5060-R	USG10R088MG-P5060-R	PDFN5x6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

 (1)Packing Type	(1) T: Tube, R: Tape Reel
 (2)Package Type	(2) TF1: TO-220F1, TN3: TO-252, P5060: PDFN5x6
 (3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

### ■ MARKING

TO-220F1 / TO-252	PDFN5×6
<p>Diagram illustrating the marking layout for a TO-220F1 or TO-252 package. The marking area contains:<ul style="list-style-type: none"><li>Top row: UTC (top left), USG10R088M (center), and a small square symbol (top right).</li><li>Middle row: A series of seven small squares representing the date code.</li><li>Bottom row: A small square representing the lot code.</li></ul>Annotations indicate:<ul style="list-style-type: none"><li>A bracket labeled "L: Lead Free" points to the small square at the top right.</li><li>A bracket labeled "G: Halogen Free" points to the small square at the bottom.</li><li>An arrow labeled "Date Code" points to the middle row of squares.</li><li>An arrow labeled "Lot Code" points to the bottom square.</li><li>The number "1" is located below the bottom square.</li></ul></p>	<p>Diagram illustrating the marking layout for a PDFN5×6 package. The marking area contains:<ul style="list-style-type: none"><li>Top row: UTC (top left), USG (top center), 10R088M (top right), and a small square symbol (middle right).</li><li>Middle row: A small square representing the lot code.</li><li>Bottom row: A series of five small squares representing the date code.</li></ul>Annotations indicate:<ul style="list-style-type: none"><li>A bracket labeled "Lot Code" points to the small square at the top right.</li><li>An arrow labeled "Date Code" points to the bottom row of squares.</li></ul></p>

■ ABSOLUTE MAXIMUM RATING (T<sub>c</sub>=25°C unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V <sub>DSS</sub>	100	V
Gate-Source Voltage		V <sub>GSS</sub>	±20	V
Drain Current	DC	I <sub>D</sub>	65	A
	Pulsed (Note 2)	I <sub>DM</sub>	130	A
Avalanche Energy	Single Pulsed (Note 3)	E <sub>AS</sub>	3.5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.3	V/ns
Power Dissipation	TO-220F1	P <sub>D</sub>	31	W
	TO-252		53	W
	PDFN5×6		43	W
Junction Temperature		T <sub>J</sub>	+150	°C
Storage Temperature Range		T <sub>STG</sub>	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. L = 0.1mH, I<sub>AS</sub> = 8.4A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C

4. I<sub>SD</sub> ≤ 30A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 25°C

## ■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220F1	θ <sub>JA</sub>	62.5	°C/W
	TO-252		110	°C/W
	PDFN5×6		65 (Note)	°C/W
Junction to Case	TO-220F1	θ <sub>JC</sub>	4.0	°C/W
	TO-252		2.36	°C/W
	PDFN5×6		2.9 (Note)	°C/W

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

# USG10R088M

**POWER MOSFET**

■ ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$  unless otherwise specified)

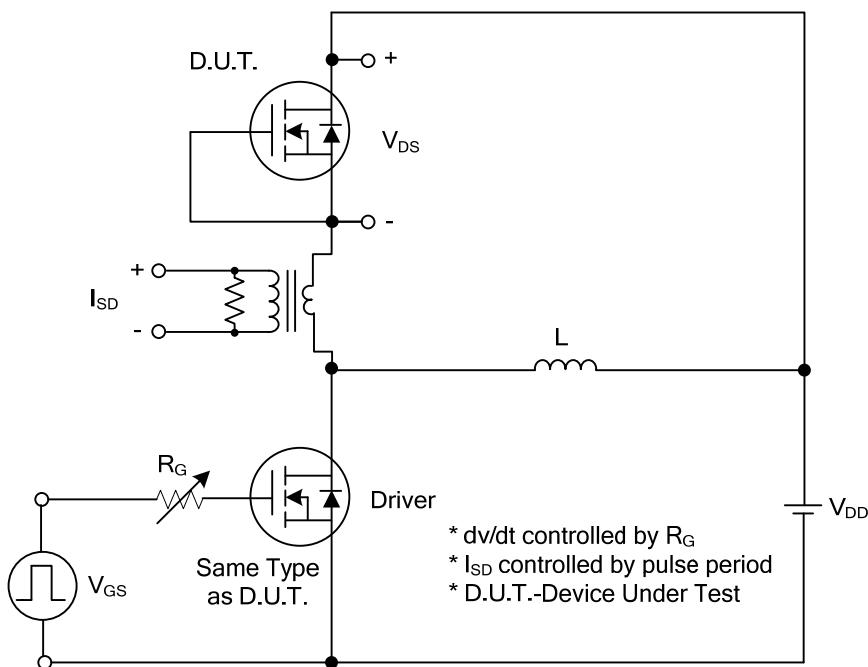
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	100			V
Drain-Source Leakage Current	$I_{\text{DS}}^{\text{SS}}$	$V_{\text{DS}}=100\text{V}, V_{\text{GS}}=0\text{V}$		1		$\mu\text{A}$
Gate-Source Leakage Current	Forward	$V_{\text{GS}}=+20\text{V}, V_{\text{DS}}=0\text{V}$			+100	nA
	Reverse	$V_{\text{GS}}=-20\text{V}, V_{\text{DS}}=0\text{V}$			-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.0		2.5	V
Static Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=32\text{A}$			8.8	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=20\text{A}$			11	$\text{m}\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=25\text{V}, f=1.0\text{MHz}$		2544		pF
Output Capacitance	$C_{\text{oss}}$			1064		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			165		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	$Q_G$	$V_{\text{DS}}=80\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=65\text{A}$ (Note 1, 2)		74		nC
Gate to Source Charge	$Q_{\text{gs}}$			9		nC
Gate to Drain Charge	$Q_{\text{gd}}$			26		nC
Turn-ON Delay Time	$t_{\text{D(ON)}}$	$V_{\text{DD}}=50\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=65\text{A},$ $R_{\text{G}}=3\Omega$ (Note 1, 2)		12		ns
Rise Time	$t_R$			20		ns
Turn-OFF Delay Time	$t_{\text{D(OFF)}}$			40		ns
Fall-Time	$t_F$			23		ns
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$				65	A
Diode Forward Voltage	$V_{\text{SD}}$	$I_F=65\text{A}, V_{\text{GS}}=0\text{V}$			1.4	V
Reverse Recovery Time (Note 1)	$t_{\text{rr}}$	$I_S=30\text{A}, V_{\text{GS}}=0\text{V},$ $dI_F/dt = 100\text{A}/\mu\text{s}$		46		nS
Reverse Recovery Charge	$Q_{\text{rr}}$			66		nC

Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

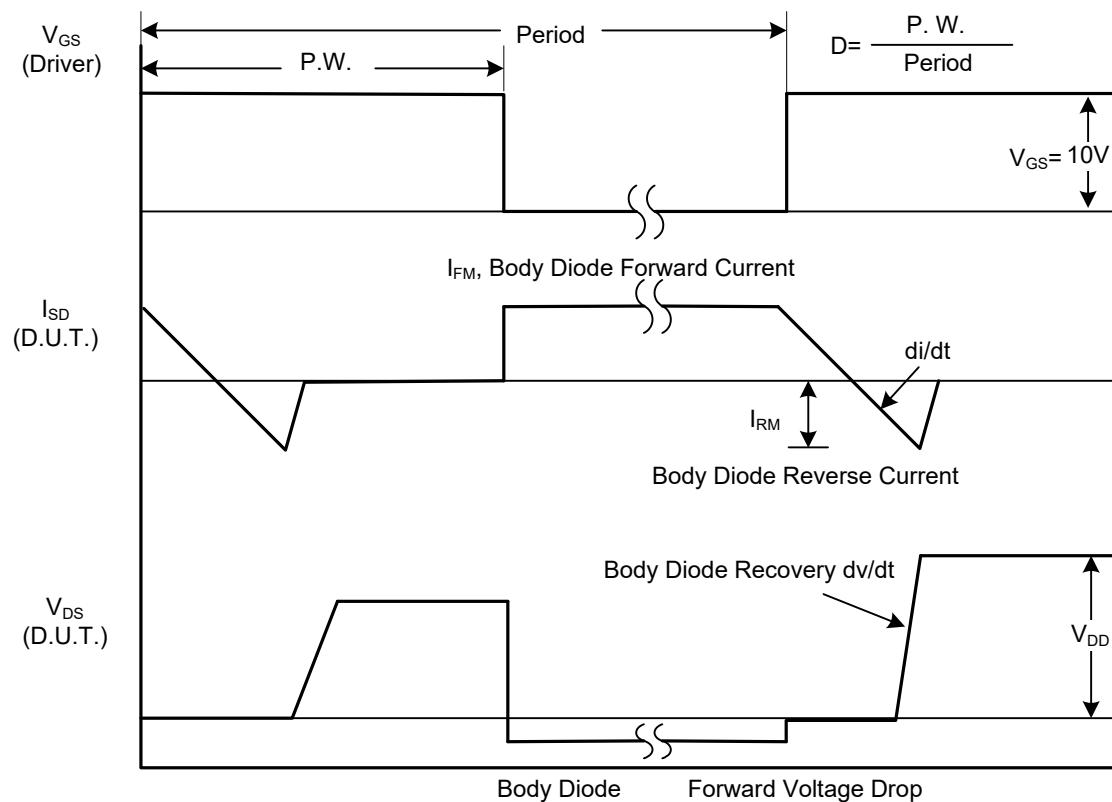
2. Essentially independent of operating temperature.



### ■ TEST CIRCUITS AND WAVEFORMS

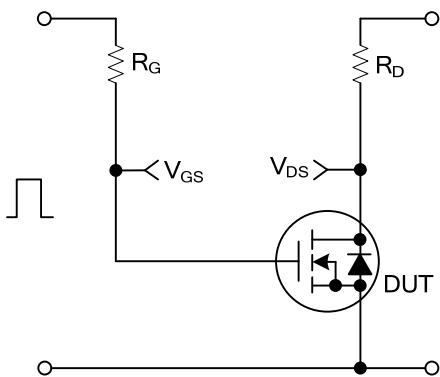


Peak Diode Recovery  $dv/dt$  Test Circuit

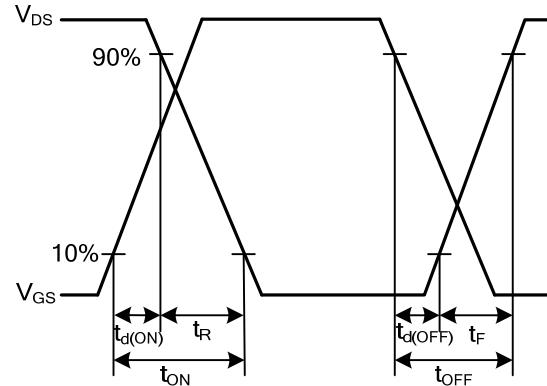


Peak Diode Recovery  $dv/dt$  Waveforms

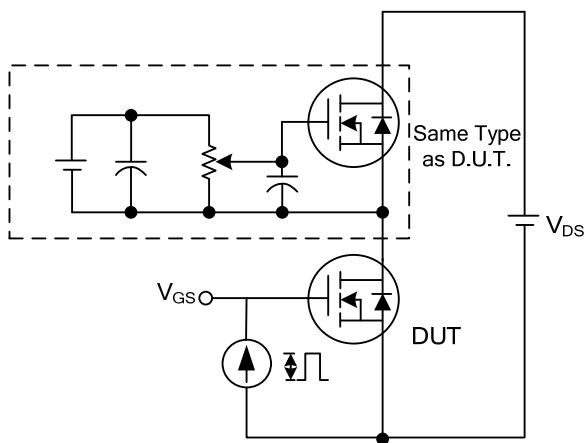
### ■ TEST CIRCUITS AND WAVEFORMS



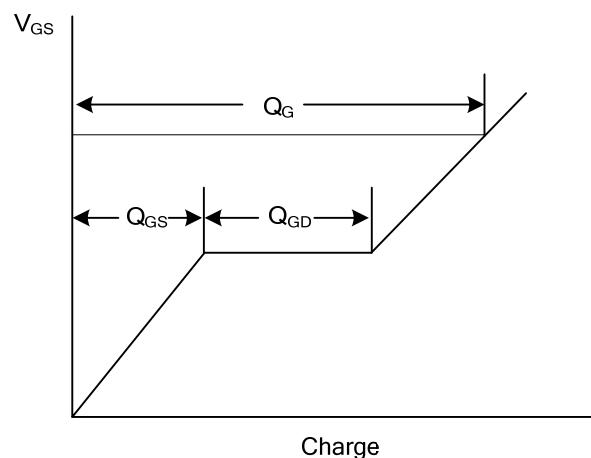
Ringing Test Circuit



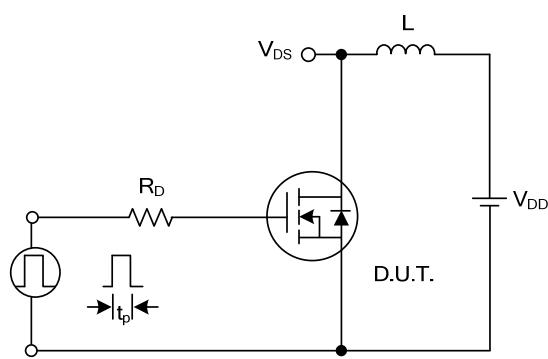
Switching Waveforms



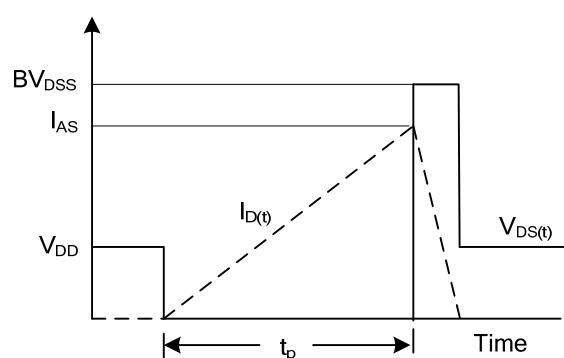
Gate Charge Test Circuit



Gate Charge Waveform

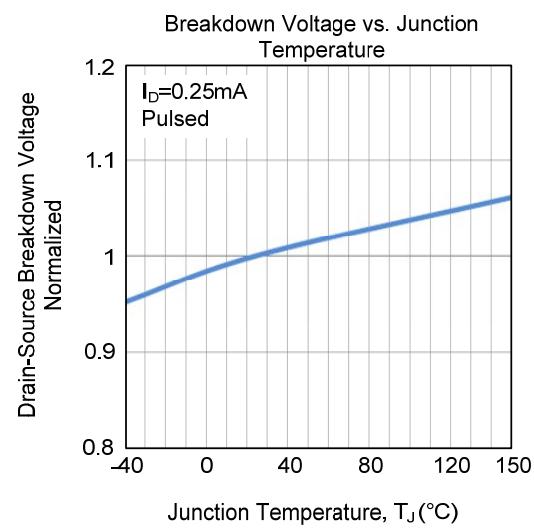
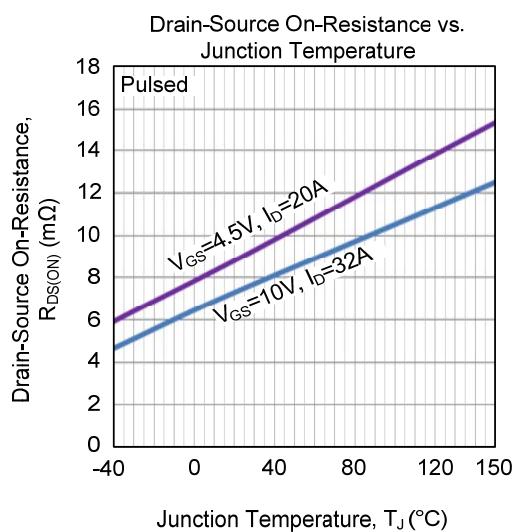
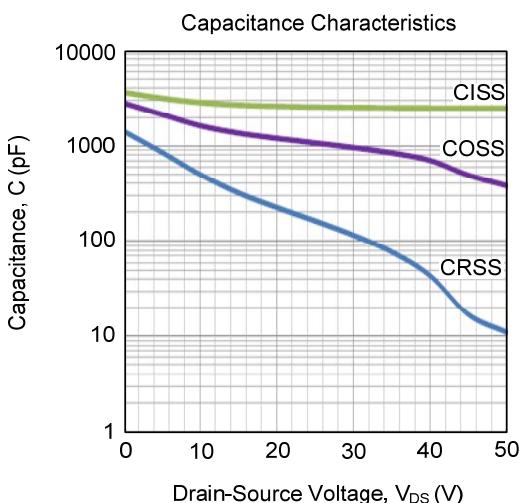
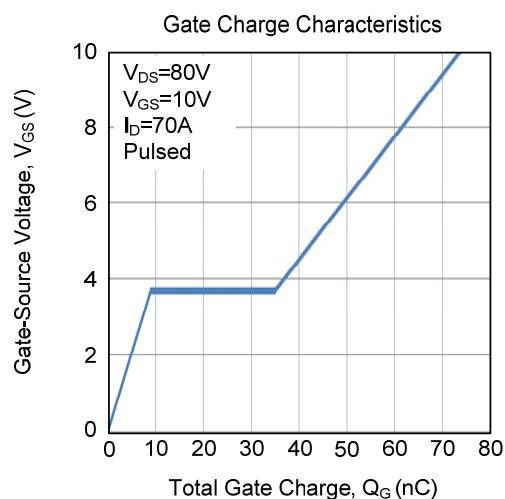
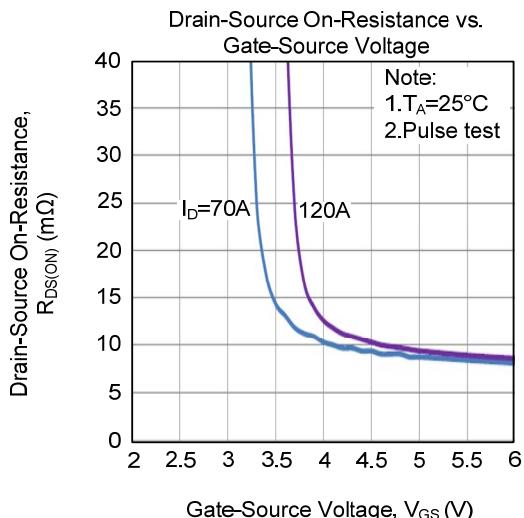
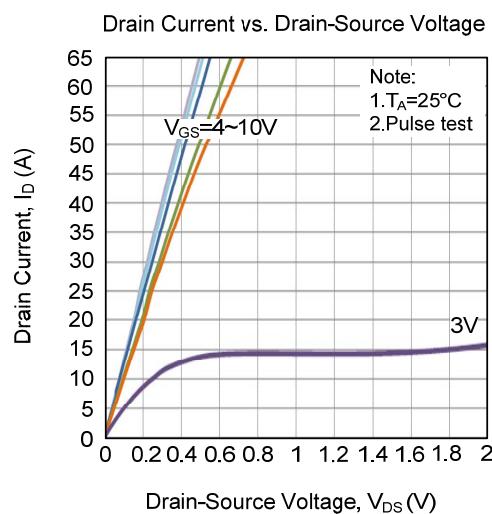


Unclamped Inductive Switching Test Circuit

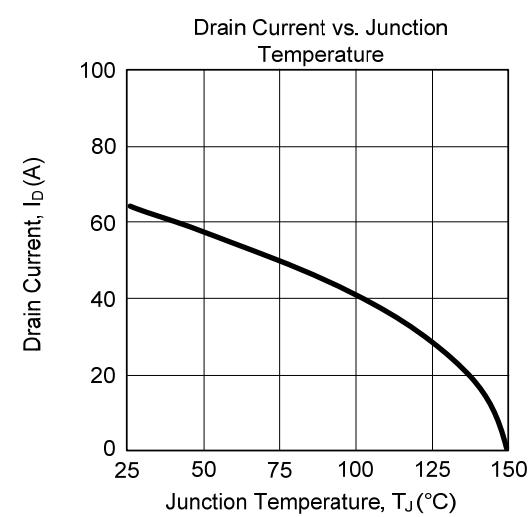
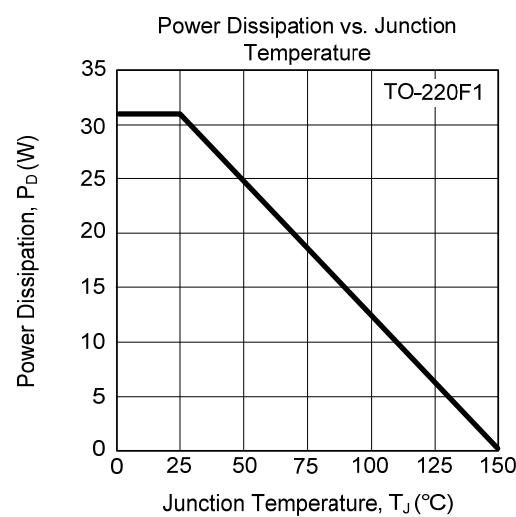
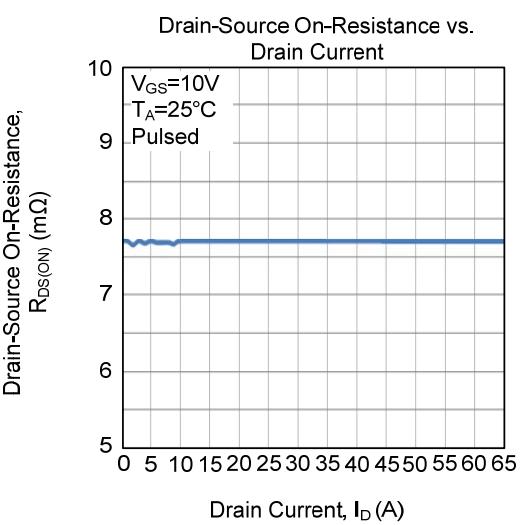
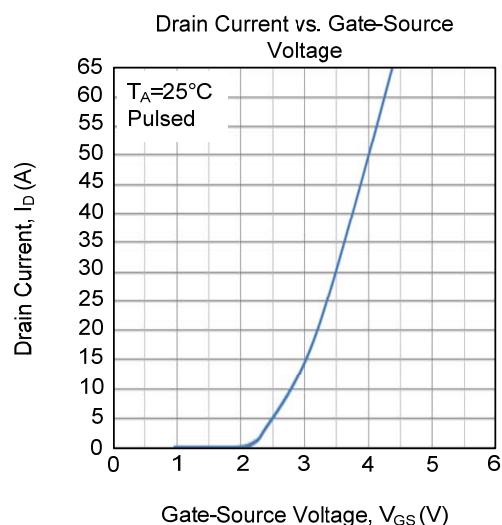
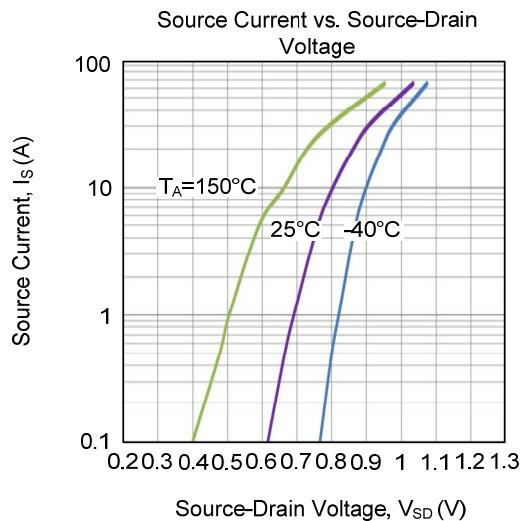
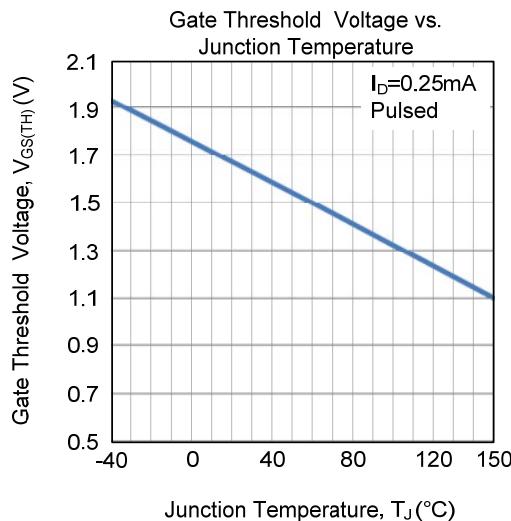


Unclamped Inductive Switching Waveforms

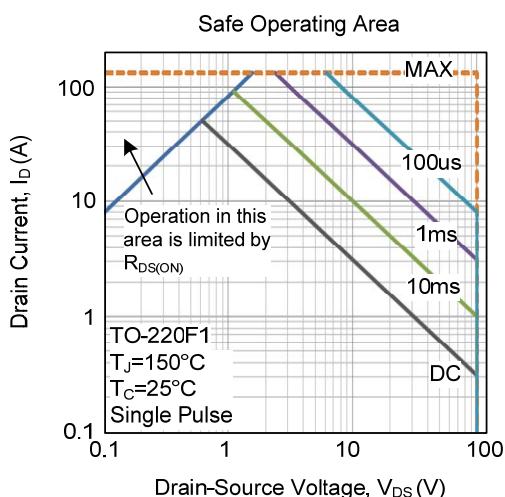
### ■ TYPICAL CHARACTERISTICS



### ■ TYPICAL CHARACTERISTICS (Cont.)



## ■ TYPICAL CHARACTERISTICS (Cont.)



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