

**UT150N03**

Preliminary

Power MOSFET

**150A, 30V N-CHANNEL
ENHANCEMENT MODE
POWER MOSFET****DESCRIPTION**

The UTC **UT150N03** uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

FEATURES**TO-220**

* $R_{DS(ON)} \leq 4.2 \text{ m}\Omega$ @ $V_{GS}=10 \text{ V}$, $I_D=50 \text{ A}$

* $R_{DS(ON)} \leq 6.0 \text{ m}\Omega$ @ $V_{GS}=4.5 \text{ V}$, $I_D=40 \text{ A}$

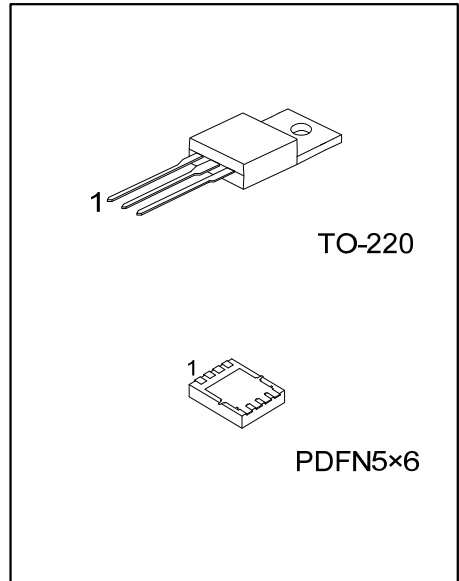
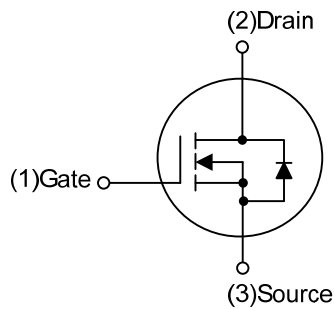
PDFN5x6

* $R_{DS(ON)} \leq 4.0 \text{ m}\Omega$ @ $V_{GS}=10 \text{ V}$, $I_D=50 \text{ A}$

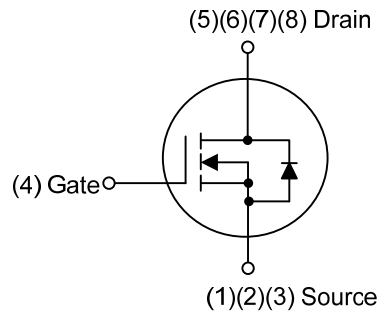
* $R_{DS(ON)} \leq 5.8 \text{ m}\Omega$ @ $V_{GS}=4.5 \text{ V}$, $I_D=40 \text{ A}$

* Excellent gate charge

* Very low on-resistance $R_{DS(ON)}$

**SYMBOL**

TO-220



PDFN5x6

ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT150N03L-TA3-T	UT150N03G-TA3-T	TO-220	G	D	S	-	-	-	-	-	Tube
UT150N03L-P5060-R	UT150N03G-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT150N03G-TA3-T (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube, R: Tape Reel (2) TA3: TO-220, P5060: PDFN5×6 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

TO-220	PDFN5×6
UTC UT150N03 Lot Code ← 1 → Date Code L: Lead Free G: Halogen Free	UTC UT 150N03 Lot Code ← • → Date Code

■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	150	A
	Pulsed (Note 2)	I_{DM}	300	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	875	mJ
Power Dissipation	TO-220	P_D	130	W
	PDFN5x6		70	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

3. $L = 0.5\text{mH}$, $I_{AS} = 35\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^{\circ}\text{C/W}$
	PDFN5x6		65 (Note)	$^{\circ}\text{C/W}$
Junction to Case	TO-220	θ_{JC}	0.96	$^{\circ}\text{C/W}$
	PDFN5x6		1.78 (Note)	$^{\circ}\text{C/W}$

Notes: 1. Maximum under Steady State conditions is 90°C/W .

2. Surface Mounted on 1" x 1" FR4 board.

■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	30			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	V
Static Drain-Source On-State Resistance	TO-220	R _{DS(ON)}	V _{GS} =10V, I _D =50A			4.2	mΩ
			V _{GS} =4.5V, I _D =40A			6.0	mΩ
	PDFN5×6		V _{GS} =10V, I _D =50A			4.0	mΩ
			V _{GS} =4.5V, I _D =40A			5.8	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		4920		pF
Output Capacitance		C _{OSS}			750		pF
Reverse Transfer Capacitance		C _{RSS}			590		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =15V, V _{GS} =10V, I _D =100A (Note 1, 2)		130		nC
Gate to Source Charge		Q _{GS}			17		nC
Gate to Drain Charge		Q _{GD}			42		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =15V, I _D =100A, R _G =3Ω V _{GS} =10V (Note 1, 2)		14		ns
Rise Time		t _R			19		ns
Turn-OFF Delay Time		t _{D(OFF)}			72		ns
Fall-Time		t _F			38		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				150	A
Maximum Body-Diode Pulsed Current		I _{SM}				300	A
Drain-Source Diode Forward Voltage		V _{SD}	I _{SD} =20A			1.5	V

Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature typical characteristics.

D.U.T.

V_{DS}

I_{SD}

L

V_{DD}

R_G

Driver

V_{GS}

Same Type as D.U.T.

- * dv/dt controlled by R_G
- * I_{SD} controlled by pulse period
- * D.U.T.-Device Under Test

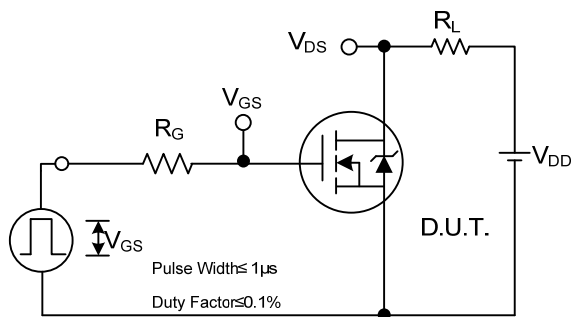
Timing diagram for a MOSFET switching a load inductor. The diagram shows three waveforms: V_{GS} (Driver), I_{SD} (D.U.T.), and V_{DS} (D.U.T.).

- V_{GS} (Driver): A square wave with period and pulse width (P.W.) indicated. The duty cycle is $D = \frac{P.W.}{Period}$. The peak voltage is $V_{GS} = 10V$.
- I_{SD} (D.U.T.): The source-drain current. It shows forward current I_{FM} (Body Diode Forward Current) during the on-state and reverse current I_{RM} (Body Diode Reverse Current) during the off-state. The reverse current is labeled I_{RM} and di/dt is indicated.
- V_{DS} (D.U.T.): The drain-source voltage. It shows the body diode forward voltage drop and the recovery dv/dt during the off-state. The peak voltage is V_{DD} .

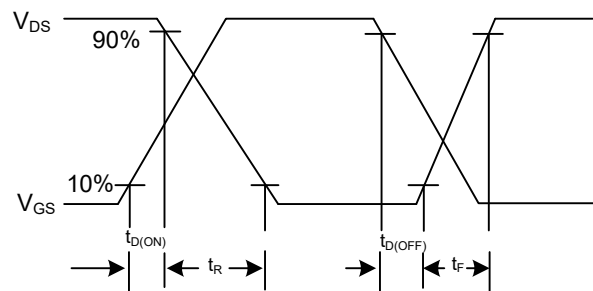
The diagram also labels the **Body Diode** and **Forward Voltage Drop**.

Peak Diode Recovery dv/dt Waveforms

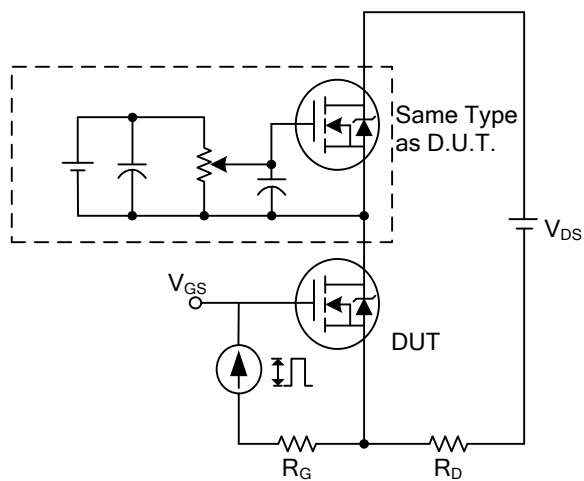
■ TEST CIRCUITS AND WAVEFORMS



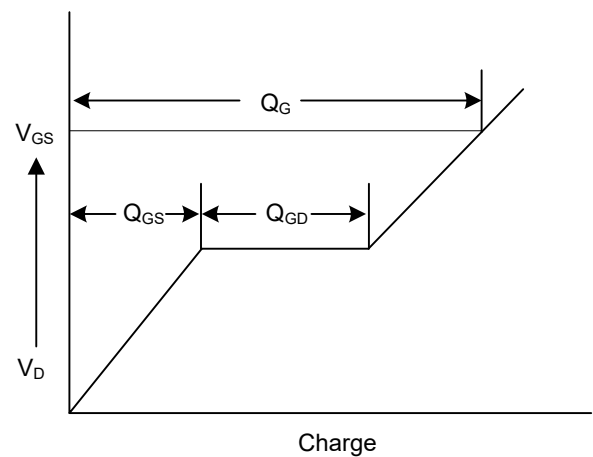
Switching Test Circuit



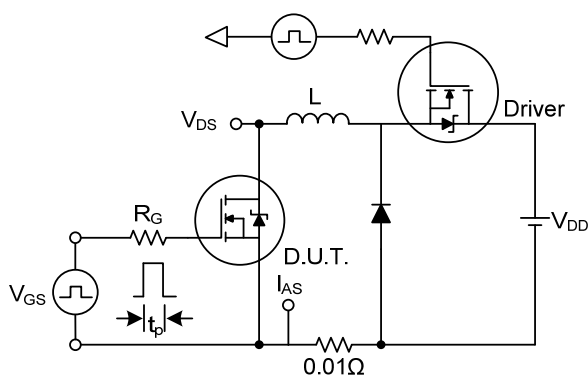
Switching Waveforms



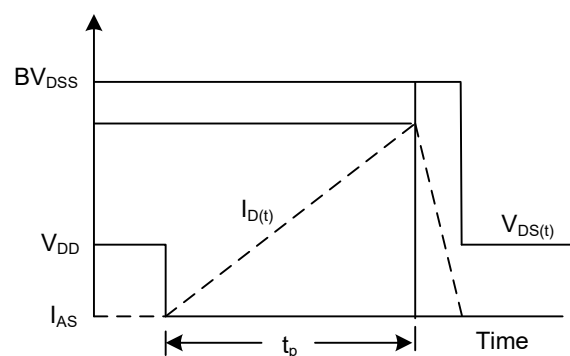
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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