

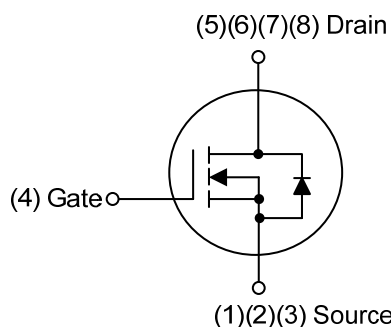
**UT20N04****POWER MOSFET****20A, 40V N-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **UT20N04** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance, low gate charge and high switching speed.

The UTC **UT20N04** is suitable for high voltage synchronous rectifier and DC/DC converters, etc.

FEATURES

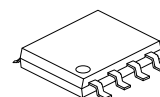
- * $R_{DS(ON)} \leq 30 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=10\text{A}$
 $R_{DS(ON)} \leq 50 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=10\text{A}$
- * High Switching Speed
- * High Cell Density Trench Technology

SYMBOL**ORDERING INFORMATION**

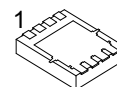
Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT20N04L-S08-R	UT20N04G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UT20N04L-P5060-R	UT20N04G-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT20N04G-S08-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) S08: SOP-8, P5060: PDFN5×6
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

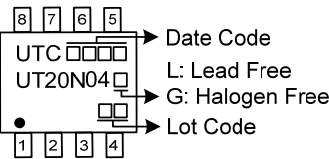
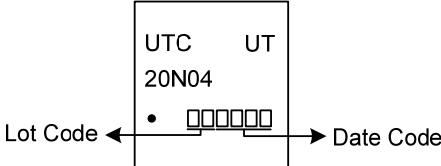


SOP-8



PDFN5×6

MARKING

SOP-8	PDFN5×6
 Diagram of SOP-8 marking: A rectangular package with pins 1-8. Markings include: Date Code (8 7 6 5), UTC, UT20N04, L (Lead Free), G (Halogen Free), and Lot Code (1 2 3 4).	 Diagram of PDFN5x6 marking: A rectangular package. Markings include: UTC, UT, 20N04, Lot Code (indicated by a dot and four squares), and Date Code (indicated by four squares).

■ ABSOLUTE MAXIMUM RATING (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	40	V
Gate-Source Voltage		V _{GSS}	±20	V
Drain Current	Continuous	I _D	20	A
	Pulsed (Note 2)	I _{DM}	40	A
Avalanche Energy (Note 3)	Single Pulsed (Note 3)	E _{AS}	72.6	mJ
Power Dissipation	SOP-8	P _D	6	W
	PDFN5×6		30	W
Junction Temperature		T _J	+150	°C
Storage Temperature Range		T _{STG}	-20 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L=30mH, I_{AS}=2.2A, V_{DD}=30V, R_G = 25Ω, Starting T_J = 25°C

4. I_{SD} ≤ 20A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ _{JA}	69.4	°C/W
	PDFN5×6		83.3	°C/W
Junction to Case	SOP-8	θ _{JC}	20.8	°C/W
	PDFN5×6		4.16	°C/W

Note: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

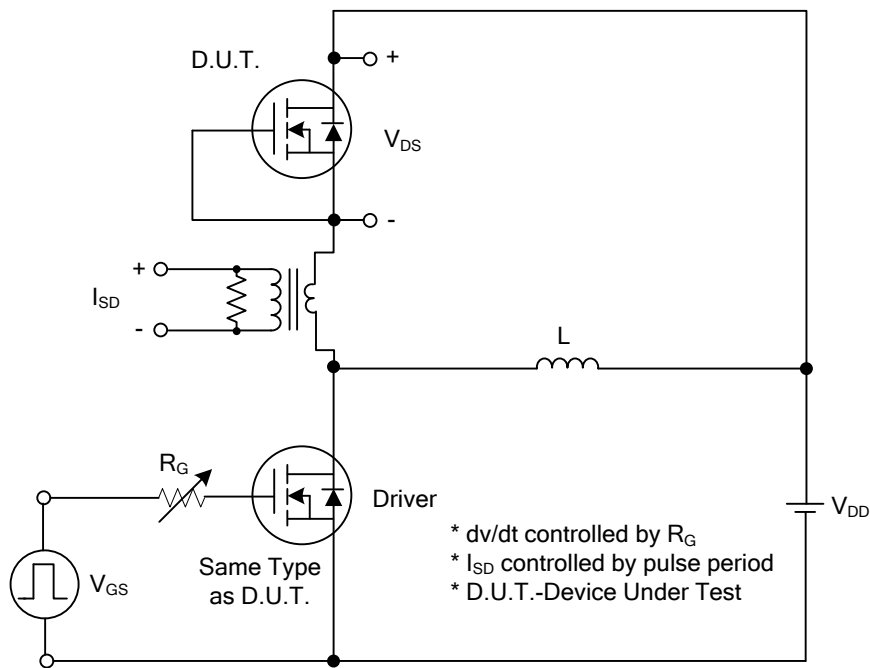
■ ELECTRICAL CHARACTERISTICS (T_J =25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =20V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =1mA	1.0		3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =10A			30	mΩ
			V _{GS} =4.5V, I _D =10A			50	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		370		pF
Output Capacitance		C _{OSS}			50		pF
Reverse Transfer Capacitance		C _{RSS}			43		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =96V, V _{GS} =10V, I _D =20A I _G =1mA (Note 1, 2)		12		nC
Gate to Source Charge		Q _{GS}			1.7		nC
Gate to Drain Charge		Q _{GD}			2		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =40V, V _{GS} =10V, I _D =20A, R _G =3Ω (Note 1, 2)		3.2		ns
Rise Time		t _R			14		ns
Turn-off Delay Time		t _{D(OFF)}			54		ns
Fall-Time		t _F			18		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				20	A
Maximum Body-Diode Pulsed Current		I _{SM}				40	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =20A, V _{GS} =0V			1.4	V

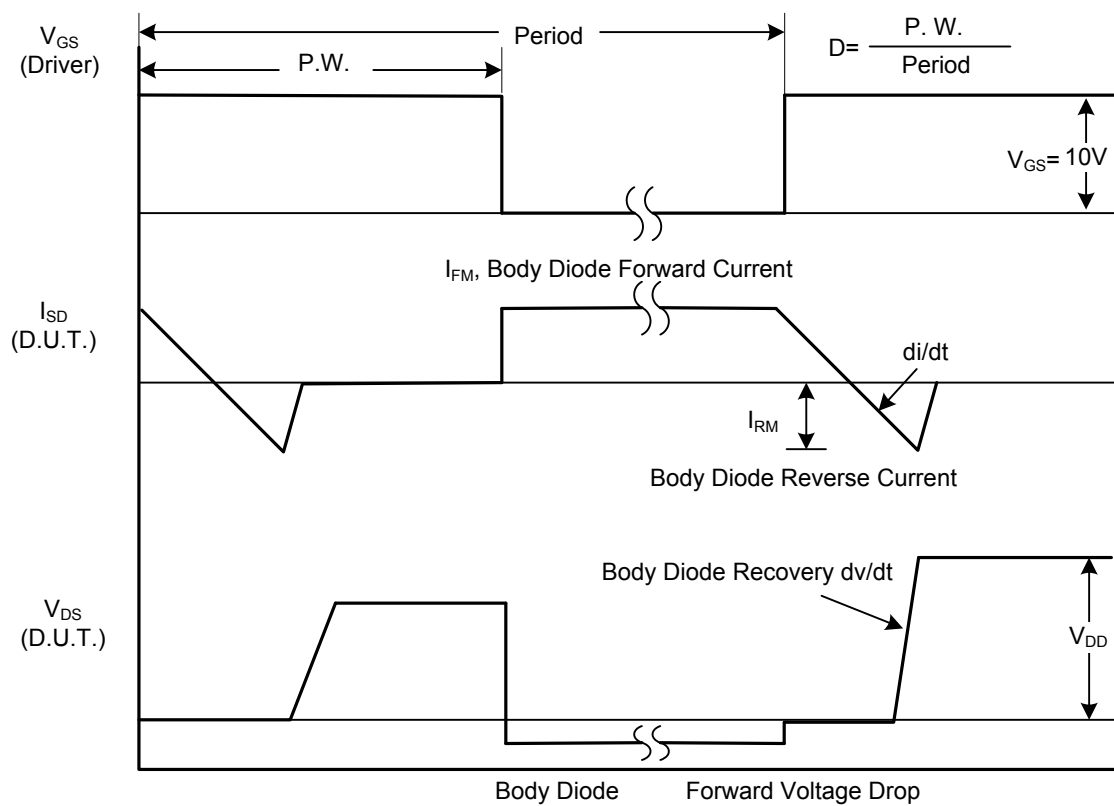
Notes: 1. Pulse Test : Pulse width ≤ 300 μs, Duty cycle ≤ 2 %.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

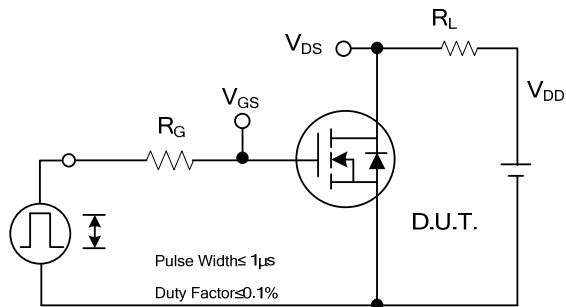


Peak Diode Recovery dv/dt Test Circuit

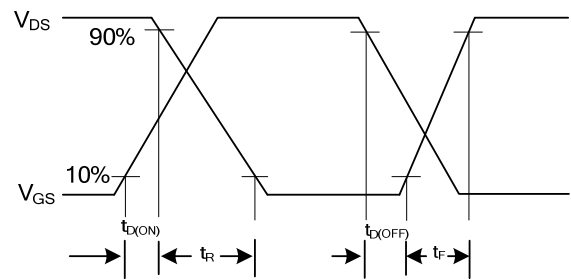


Peak Diode Recovery dv/dt Waveforms

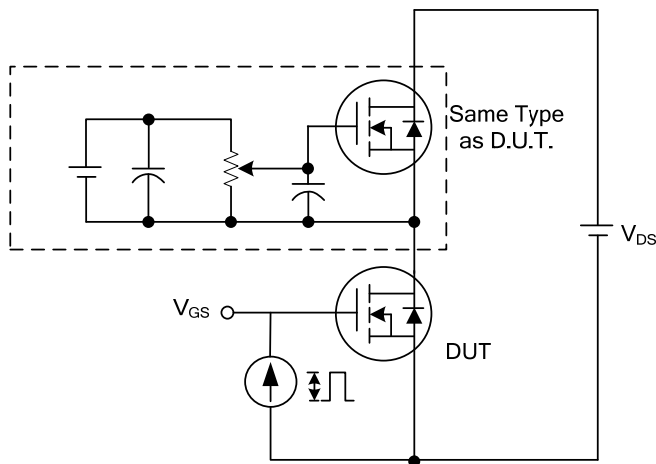
■ TEST CIRCUITS AND WAVEFORMS



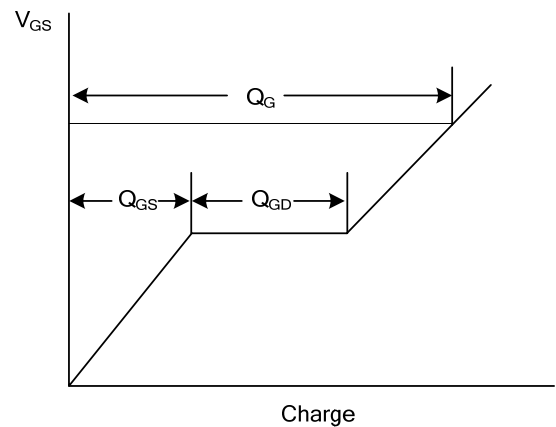
Switching Test Circuit



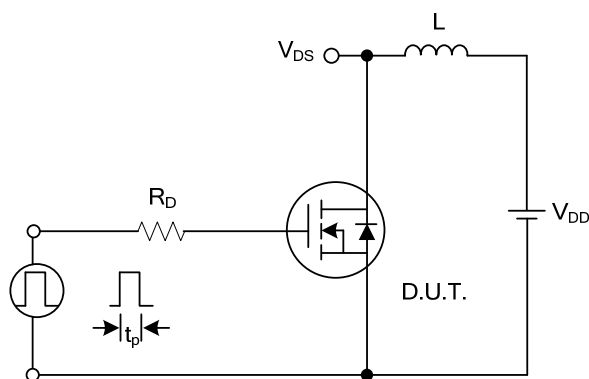
Switching Waveforms



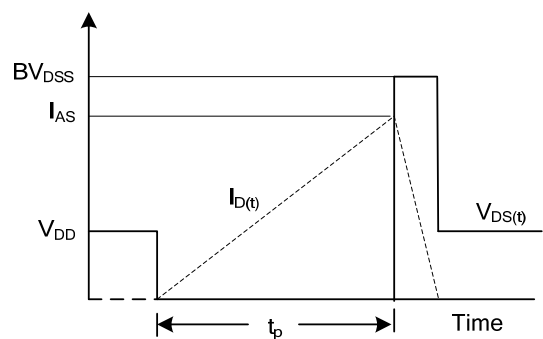
Gate Charge Test Circuit



Gate Charge Waveform

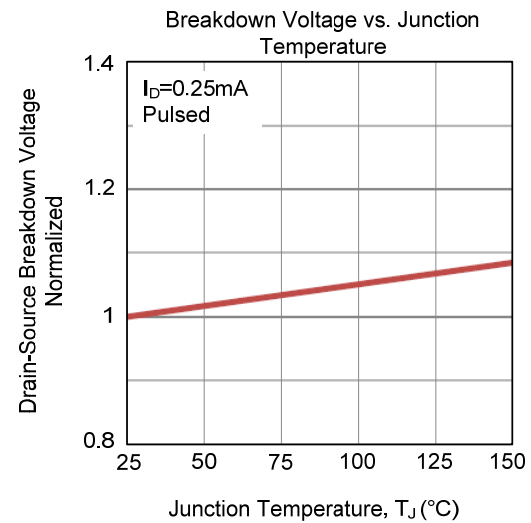
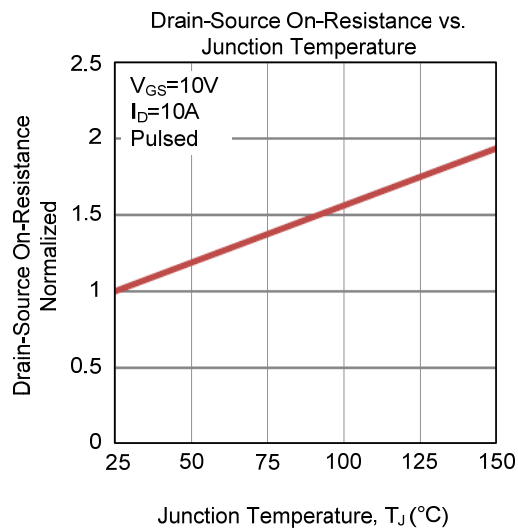
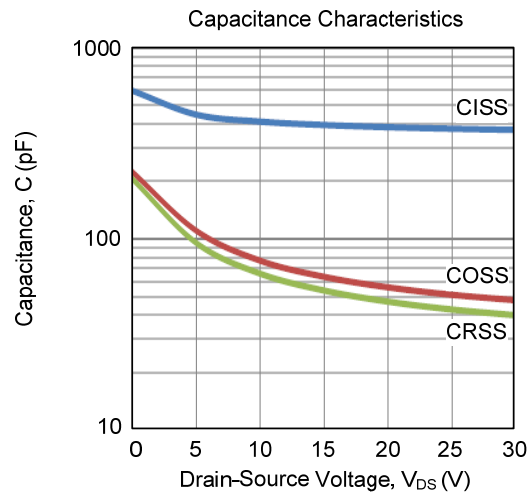
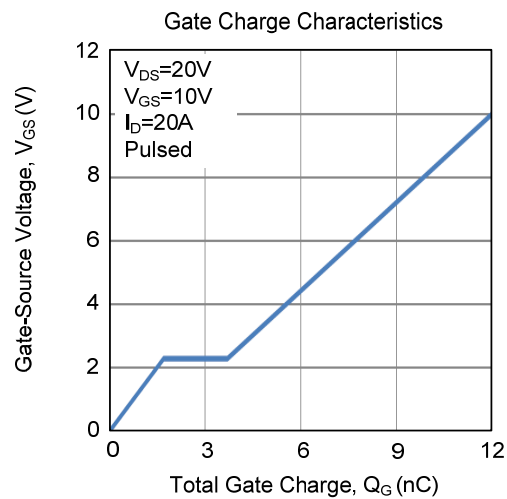
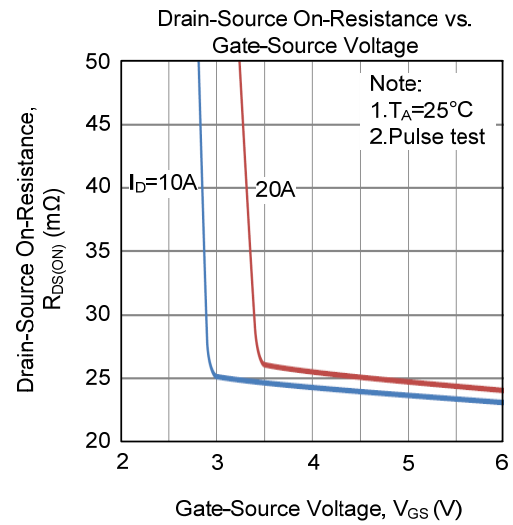
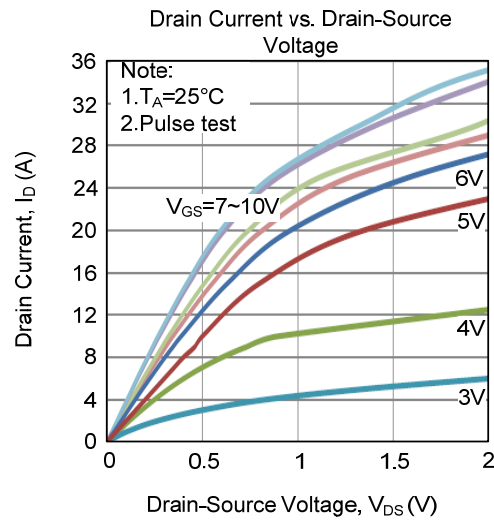


Unclamped Inductive Switching Test Circuit

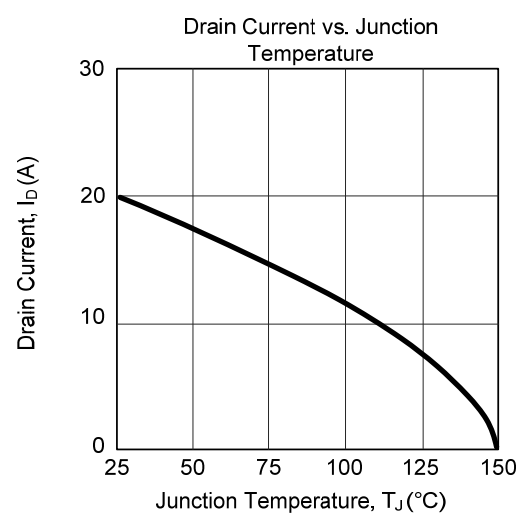
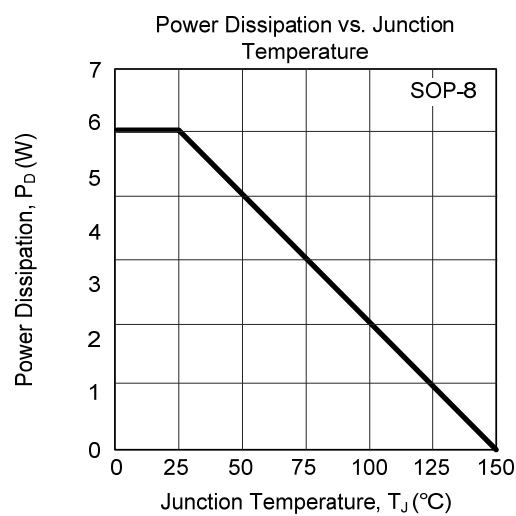
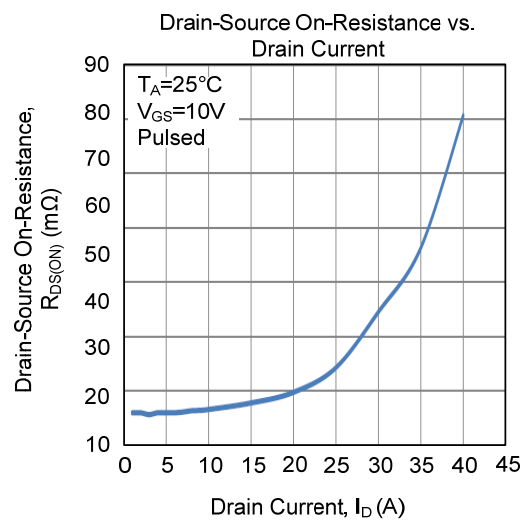
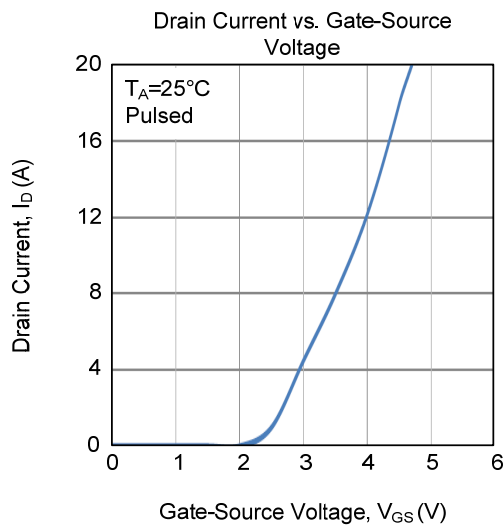
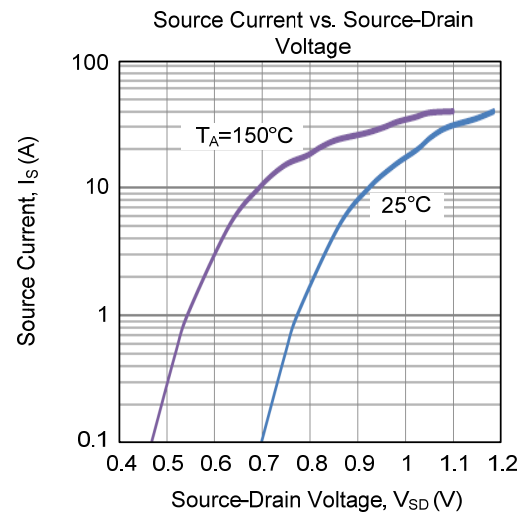
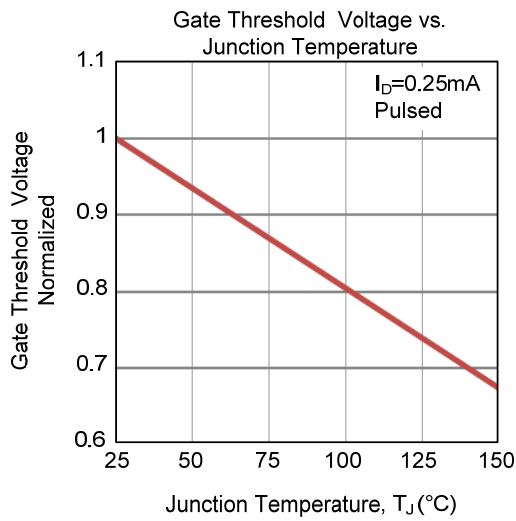


Unclamped Inductive Switching Waveforms

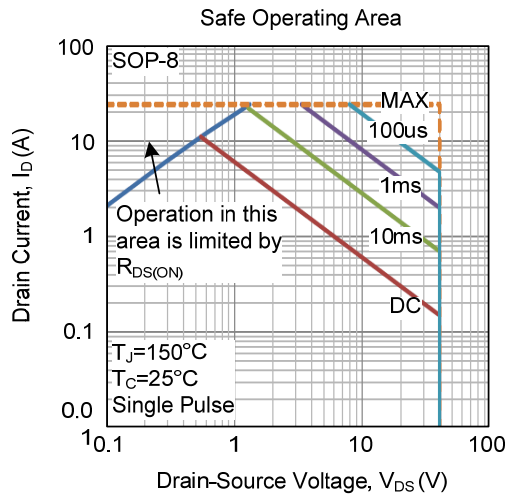
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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