



## UT2P20

Preliminary

Power MOSFET

### -2.0A, -200V P-CHANNEL POWER MOSFET

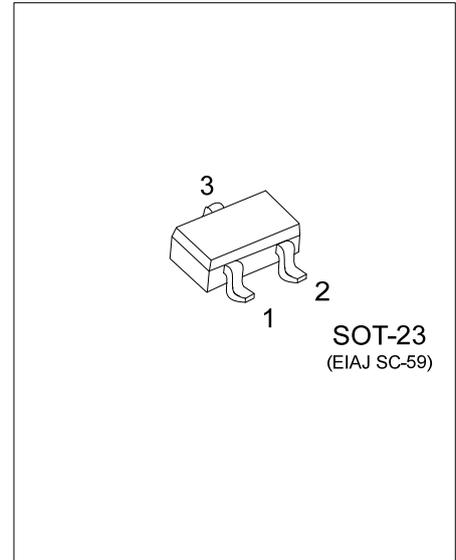
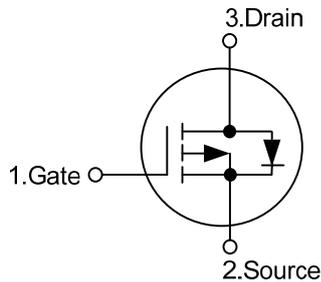
#### DESCRIPTION

The UTC **UT2P20** is a P-channel mode power MOSFET using UTC's advanced technology process to minimize on state resistance and yet maintain low gate charge for superior switching performance. Applicable at portable electronics, load switching, power management, battery charging circuits and DC to DC conversion.

#### FEATURES

- \*  $R_{DS(ON)} \leq 3.0 \Omega @ V_{GS}=-10V, I_D=-1.0A$
- \*  $R_{DS(ON)} \leq 4.0 \Omega @ V_{GS}=-4.5V, I_D=-1.0A$
- \* Low gate charge

#### SYMBOL



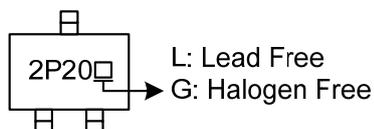
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT2P20L-AE3-R	UT2P20G-AE3-R	SOT-23	G	S	D	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain

<p>UT2P20G-AE3-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) AE3: SOT-23</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	$V_{DSS}$	-200	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current	Continuous	$I_D$	-2
	Pulsed	$I_{DM}$	-4
Peak Diode Recovery dv/dt (Note 3)	dv/dt	8.2	V/ns
Power Dissipation (Note 1, 2)	$P_D$	0.35	W
Junction Temperature	$T_J$	+150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $I_{SD} \leq -2.0\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J = 25^\circ\text{C}$ .

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	350	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

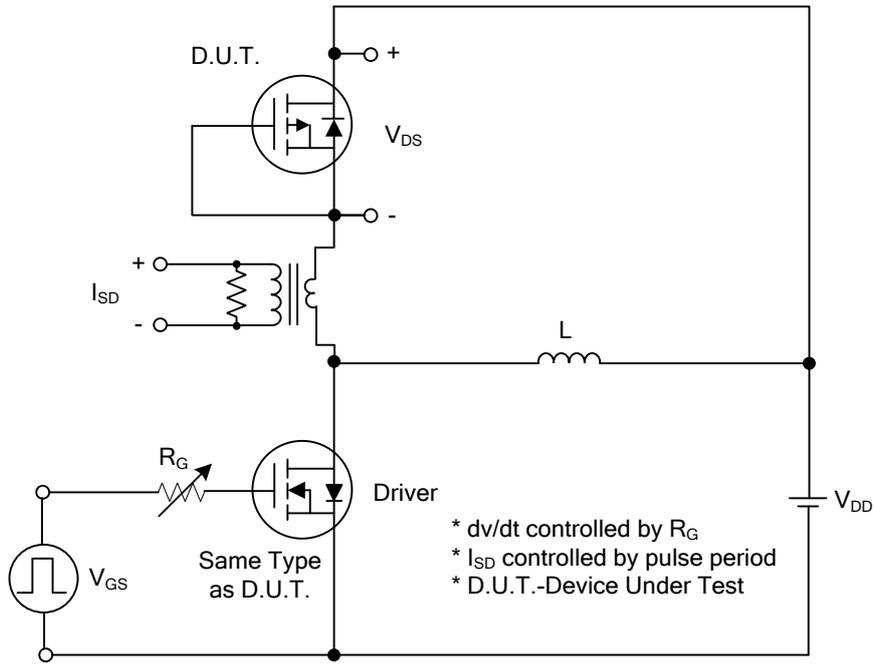
■ ELECTRICAL CHARACTERISTICS ( $T_J=25^\circ\text{C}$  unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0\text{V}$ , $I_D=-250\mu\text{A}$	-200			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=-200\text{V}$ , $V_{GS}=0\text{V}$			-1	$\mu\text{A}$
Gate-Source Leakage Current	Forward	$I_{GSS}$			+100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=-250\mu\text{A}$	-1.0		-3.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10\text{V}$ , $I_D=-1.0\text{A}$			3.0	$\Omega$
		$V_{GS}=-4.5\text{V}$ , $I_D=-1.0\text{A}$			4.0	$\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=-25\text{V}$ , $f=1.0\text{MHz}$		262		pF
Output Capacitance	$C_{OSS}$			24		pF
Reverse Transfer Capacitance	$C_{RSS}$			10		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	$Q_G$	$V_{DS}=-100\text{V}$ , $V_{GS}=-10\text{V}$ , $I_D=-2\text{A}$ , $I_G=-1\text{mA}$ (Note 1, 2)		11		nC
Gate to Source Charge	$Q_{GS}$			3		nC
Gate to Drain Charge	$Q_{GD}$			1.9		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=-100\text{V}$ , $V_{GS}=-10\text{V}$ , $I_D=-2\text{A}$ , $R_G=6\Omega$ (Note 1, 2)		4.8		ns
Rise Time	$t_R$			17		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			14		ns
Fall-Time	$t_F$			19		ns
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$				-2	A
Maximum Pulsed Drain-Source Diode Forward Current	$I_{SM}$				-4	A
Diode Forward Voltage	$V_{SD}$	$I_F=-2.0\text{A}$ , $V_{GS}=0\text{V}$			-1.4	V
Reverse Recovery Time	$t_{rr}$	$I_S=-2.0\text{A}$ , $V_{GS}=0\text{V}$		64		ns
Reverse Recovery Charge	$Q_{rr}$	$dI_F/dt=-100\text{A}/\mu\text{s}$ (Note 1)		149		nC

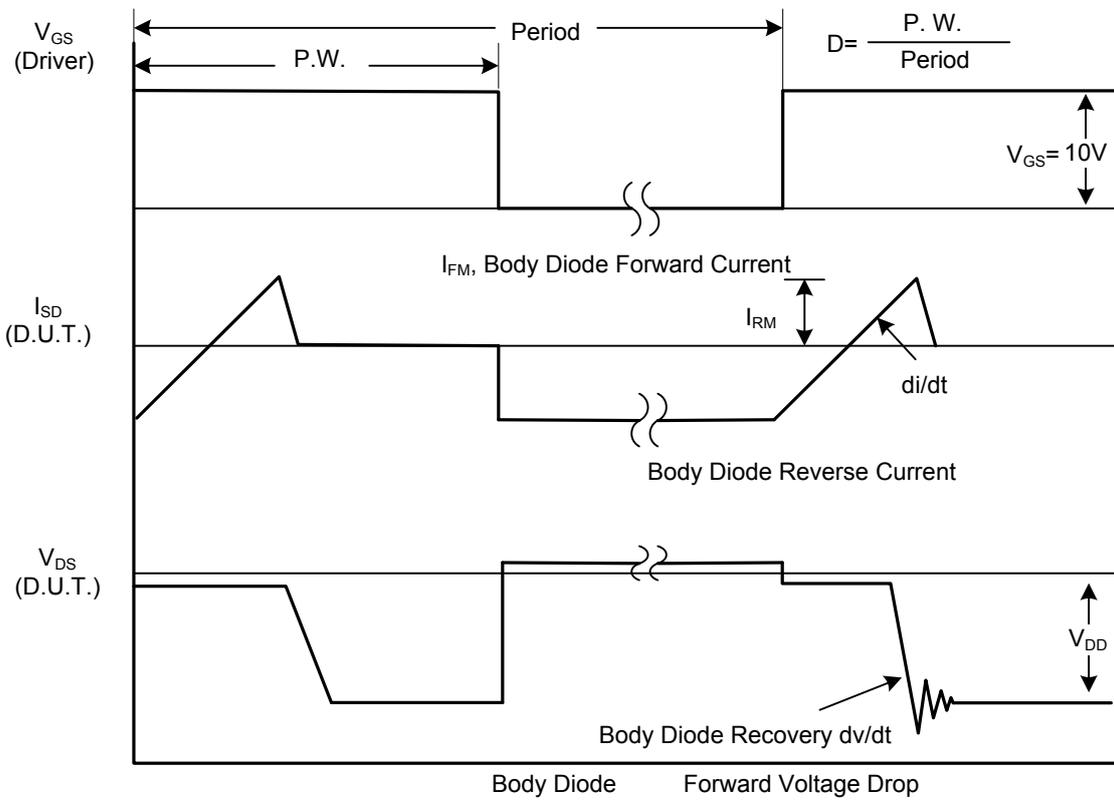
Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

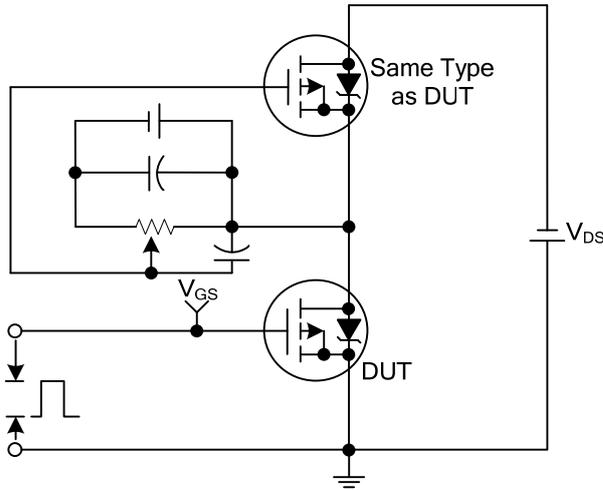


Peak Diode Recovery  $dv/dt$  Test Circuit

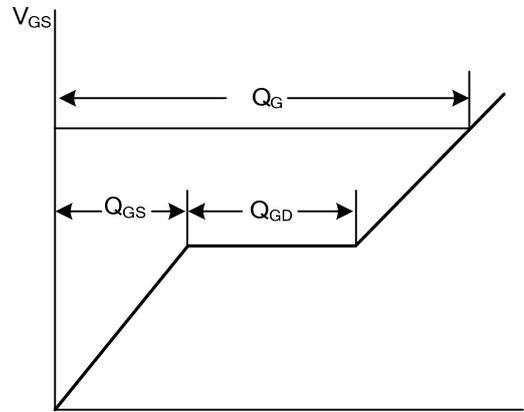


Peak Diode Recovery  $dv/dt$  Waveforms

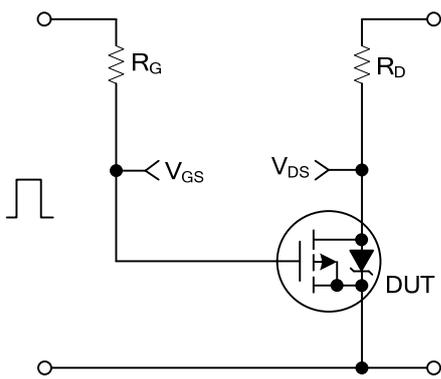
■ TEST CIRCUITS AND WAVEFORMS



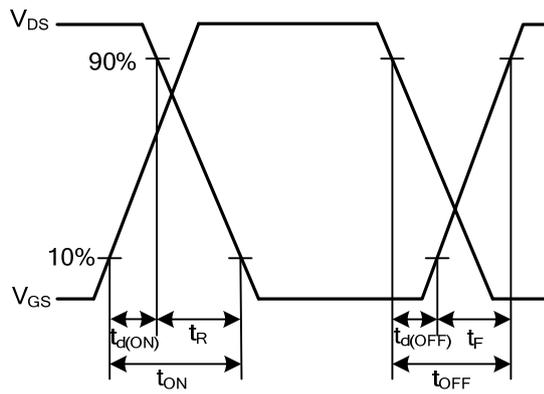
Gate Charge Test Circuit



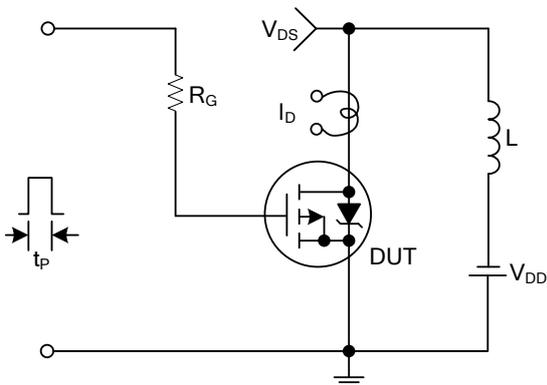
Gate Charge Waveforms



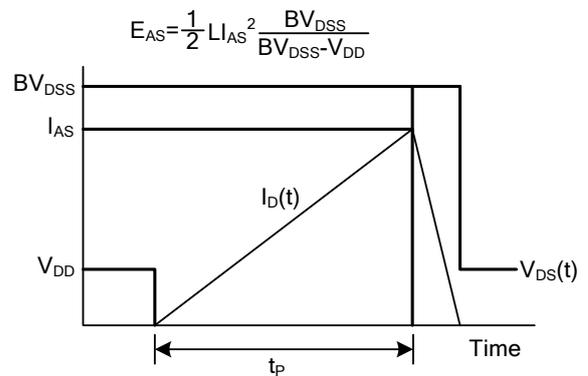
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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