



UT30N07

Preliminary

Power MOSFET

30A, 70V N-CHANNEL POWER MOSFET

DESCRIPTION

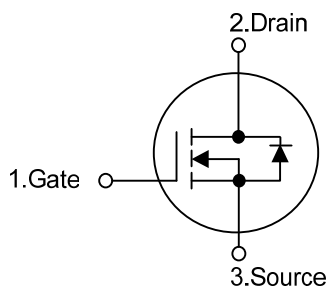
The UTC **UT30N07** is a N-channel enhancement MOSFET using UTC's advanced technology to provide the customers with perfect $R_{DS(ON)}$ and high switching speed.

The UTC **UT30N07** is suitable for all commercial-industrial applications at power dissipation levels to approximately 50 watts, etc.

FEATURES

- * $R_{DS(ON)} \leq 19 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=15\text{A}$
- $R_{DS(ON)} \leq 23 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=15\text{A}$
- * High Switching Speed

SYMBOL



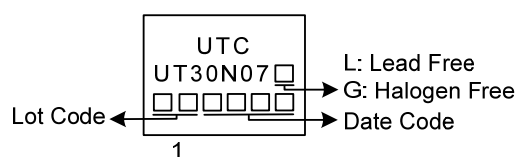
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT30N07L-TM3-T	UT30N07G-TM3-T	TO-251	G	D	S	Tube
UT30N07L-TN3-R	UT30N07G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

		<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TM3: TO-251, TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	70	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous ($V_{GS}=10V$)	I_D	30	A
	Pulsed (Note 2)	I_{DM}	60	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	28.3	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.1	V/ns
Power Dissipation		P_D	50	W
Junction Temperature		T_J	+150	$^{\circ}C$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}C$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1mH$, $I_{AS}=23.8A$, $V_{DD}=50V$, $R_G=25\Omega$, Starting $T_J=25^{\circ}C$

4. $I_{SD} \leq 30A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}C$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}C/W$
Junction to Case	θ_{JC}	2.5 (Note)	$^{\circ}C/W$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

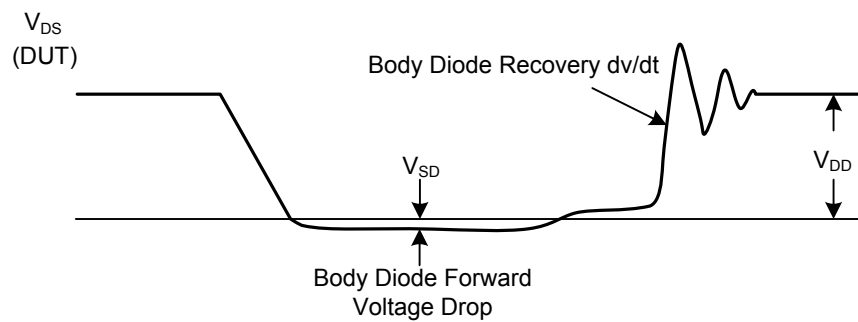
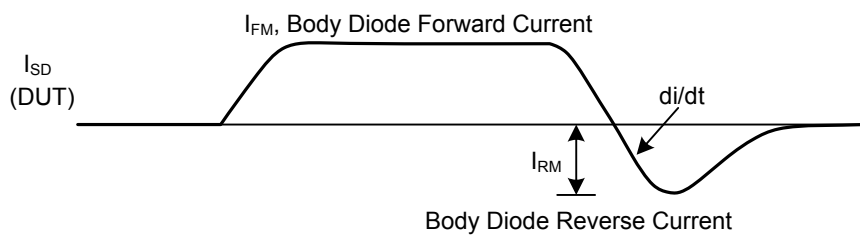
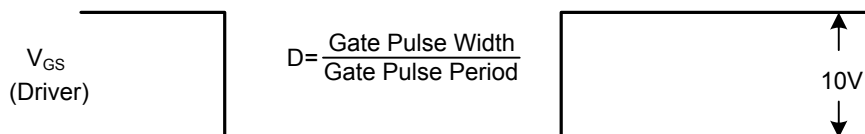
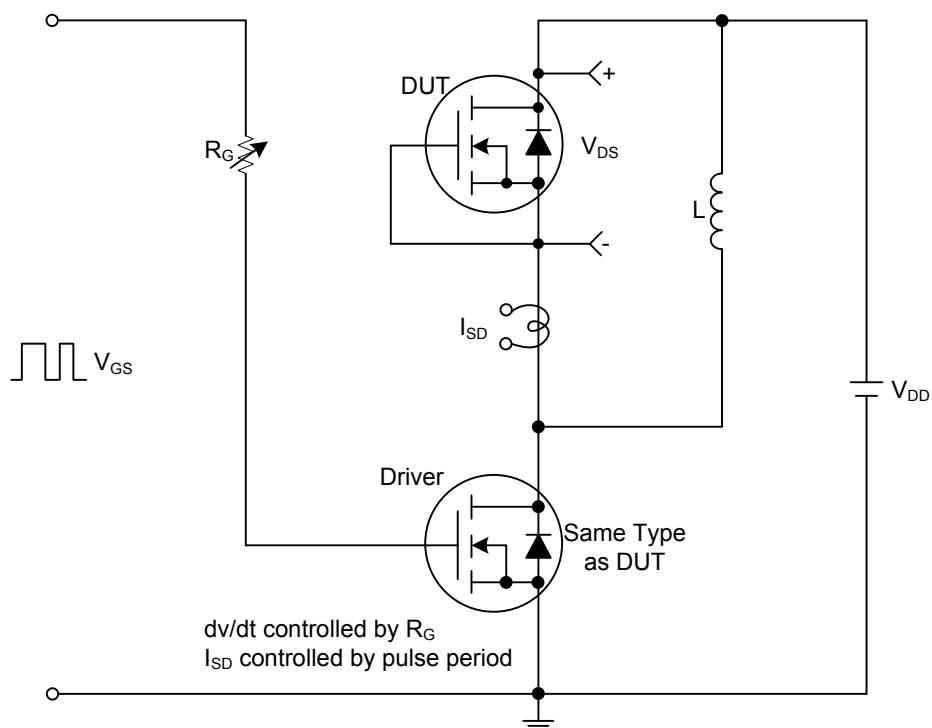
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	70			V
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=70V, V_{GS}=0V$			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+20V, V_{DS}=0V$			+100	nA
	Reverse		$V_{GS}=-20V, V_{DS}=0V$			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=10V, I_D=15A$			19	m Ω
			$V_{GS}=4.5V, I_D=15A$			23	m Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$		1263		pF
Output Capacitance		C_{OSS}			143		pF
Reverse Transfer Capacitance		C_{RSS}			109.7		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	$V_{DS}=56V, V_{GS}=10V, I_D=30A$ $I_G=1mA$ (Note 2)		39.6		nC
Gate to Source Charge		Q_{GS}			4.8		nC
Gate to Drain Charge		Q_{GD}			11.2		nC
Turn-ON Delay Time		$t_{D(ON)}$	$V_{DD}=70V, V_{GS}=10V, I_D=30A,$ $R_G=6\Omega,$ (Note 2)		7.4		ns
Rise Time		t_R			18.4		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			36.4		ns
Fall-Time		t_F			20.9		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I_S				30	A
Maximum Pulsed Drain-Source Diode Forward Current		I_{SM}				60	A
Drain-Source Diode Forward Voltage		V_{SD}	$I_S=30A, V_{GS}=0V$			1.4	V
Body Diode Reverse Recovery Time		t_{rr}	$I_F=30A, V_{GS}=0V, di/dt=100A/\mu s$		36		ns
Body Diode Reverse Recovery Charge		Q_{rr}			71.6		nC

Notes: 1. Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

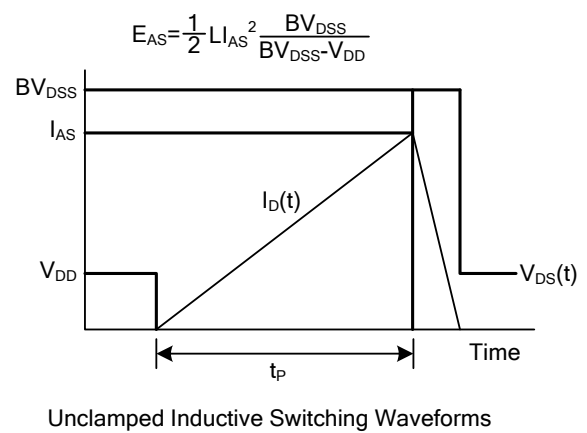
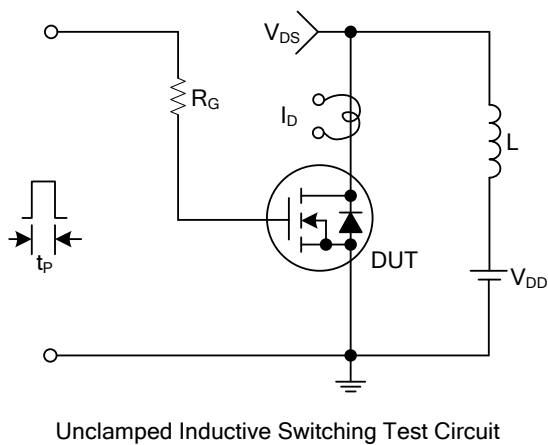
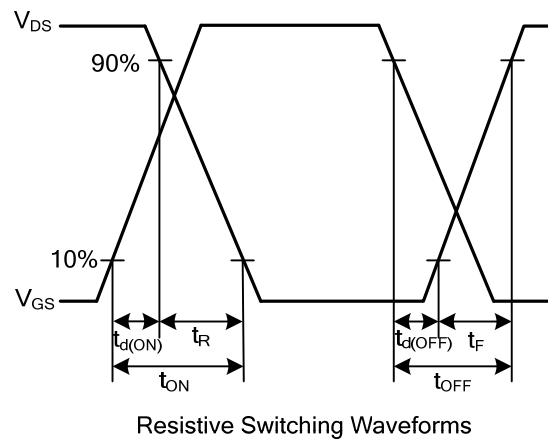
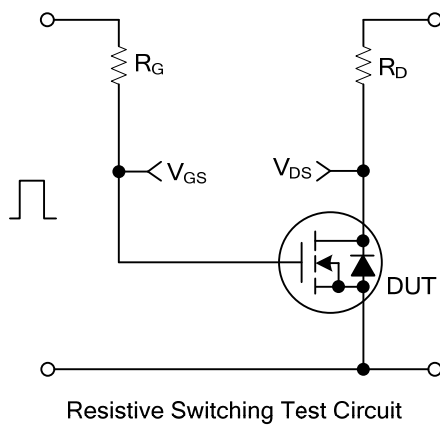
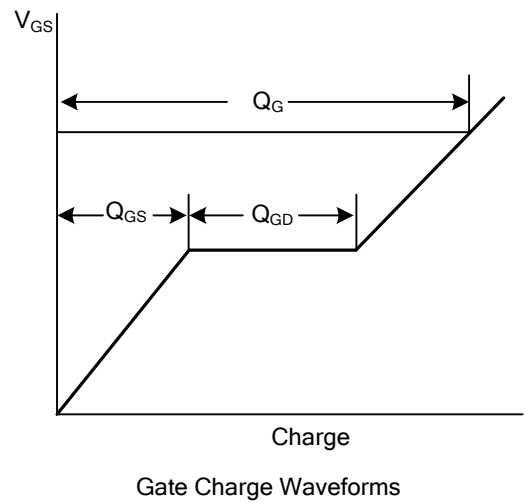
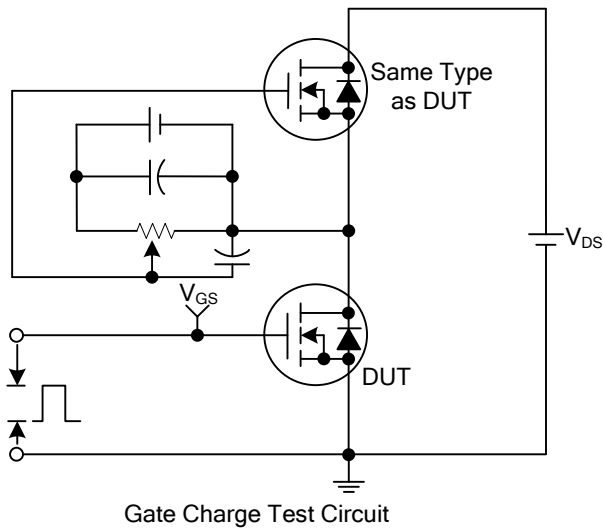
2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit and Waveforms

■ TEST CIRCUITS AND WAVEFORMS



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