



UT35P06M

Preliminary

POWER MOSFET

-35A, -60V P-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **UT35P06M** is P-channel enhancement mode power MOSFET using UTC's advanced technology to provide customers with ideal for low voltage inverter applications.

The UTC **UT35P06M** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

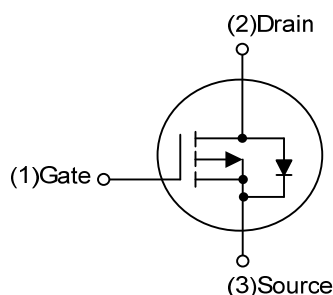
* $R_{DS(ON)} \leq 35 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$, $I_D = -15\text{A}$

$R_{DS(ON)} \leq 40 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -10\text{A}$

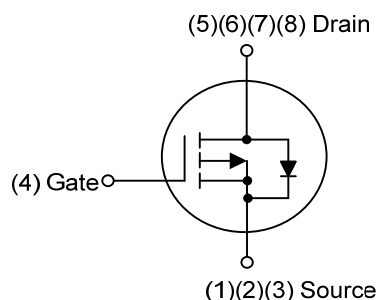
* High Cell Density Trench Technology

* High Power and Current Handling Capability

SYMBOL



TO-252



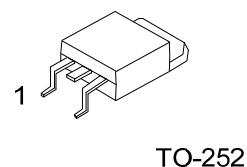
PDFN3x3

ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT35P06ML-TN3-R	UT35P06MG-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UT35P06ML-P3030-R	UT35P06MG-P3030-R	PDFN3x3	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT35P06MG-TN3-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) TN3: TO-252, P3030: PDFN3x3
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

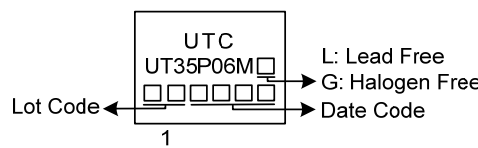
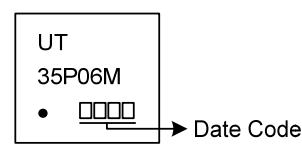


TO-252



PDFN3x3

MARKING

TO-252	PDFN3x3
 Diagram of TO-252 marking: A rectangular package with 'UTC' and 'UT35P06M' printed on top. Below the part number are four small squares. An arrow points from the left to the first square, labeled 'Lot Code'. An arrow points from the right to the last square, labeled 'Date Code'. To the right of the package, text indicates 'L: Lead Free' and 'G: Halogen Free'. A small square is shown to the right of the part number. A '1' is printed below the package.	 Diagram of PDFN3x3 marking: A square package with 'UT' and '35P06M' printed on top. Below the part number are four small squares. An arrow points from the right to the last square, labeled 'Date Code'. A small circle is shown to the left of the squares.

■ ABSOLUTE MAXIMUM RATING ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	-60	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current ($T_C=25^{\circ}\text{C}$)	Continuous	I_D	-35	A
	Pulsed (Note 2)	I_{DM}	-70	A
Avalanche Energy (Note 3)	Single Pulsed (Note 3)	E_{AS}	28	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.7	V/nS
Power Dissipation ($T_C=25^{\circ}\text{C}$)	TO-252	P_D	45	W
	PDFN3×3		36	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L = 0.1\text{mH}$, $I_{AS} = -24\text{A}$, $V_{DD} = -50\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq -30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
	PDFN3×3		75	
Junction to Case	TO-252	θ_{JC}	2.77	$^{\circ}\text{C}/\text{W}$
	PDFN3×3		3.47	

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

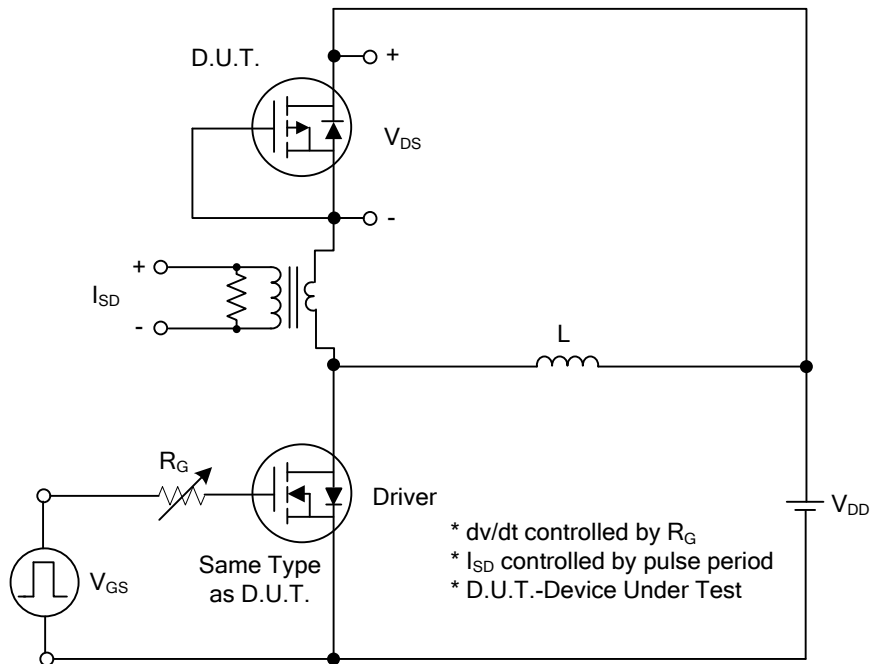
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =-250μA, V _{GS} =0V	-60			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =-60V, V _{GS} =0V, T _J =25°C			-1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =-10V, I _D =-15A			35	mΩ
			V _{GS} =-4.5V, I _D =-10A			40	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz		2060		pF
Output Capacitance		C _{OSS}			165		pF
Reverse Transfer Capacitance		C _{RSS}			130		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =-48V, V _{GS} =-10V, I _D =-35A (Note 1, 2)		38		nC
Gate to Source Charge		Q _{GS}			5.5		nC
Gate to Drain Charge		Q _{GD}			9		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =-30V, V _{GS} =-10V, I _D =-35A, R _G =3Ω (Note 1, 2)		6		ns
Rise Time		t _R			18		ns
Turn-off Delay Time		t _{D(OFF)}			58		ns
Fall-Time		t _F			28		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				-35	A
Maximum Body-Diode Pulsed Current		I _{SM}				-70	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =-35A, V _{GS} =0V			-1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =-30A, V _{GS} =0V,		45		ns
Reverse Recovery Charge		Q _{rr}	di _F /dt=100A/μs (Note 1)		32		ns

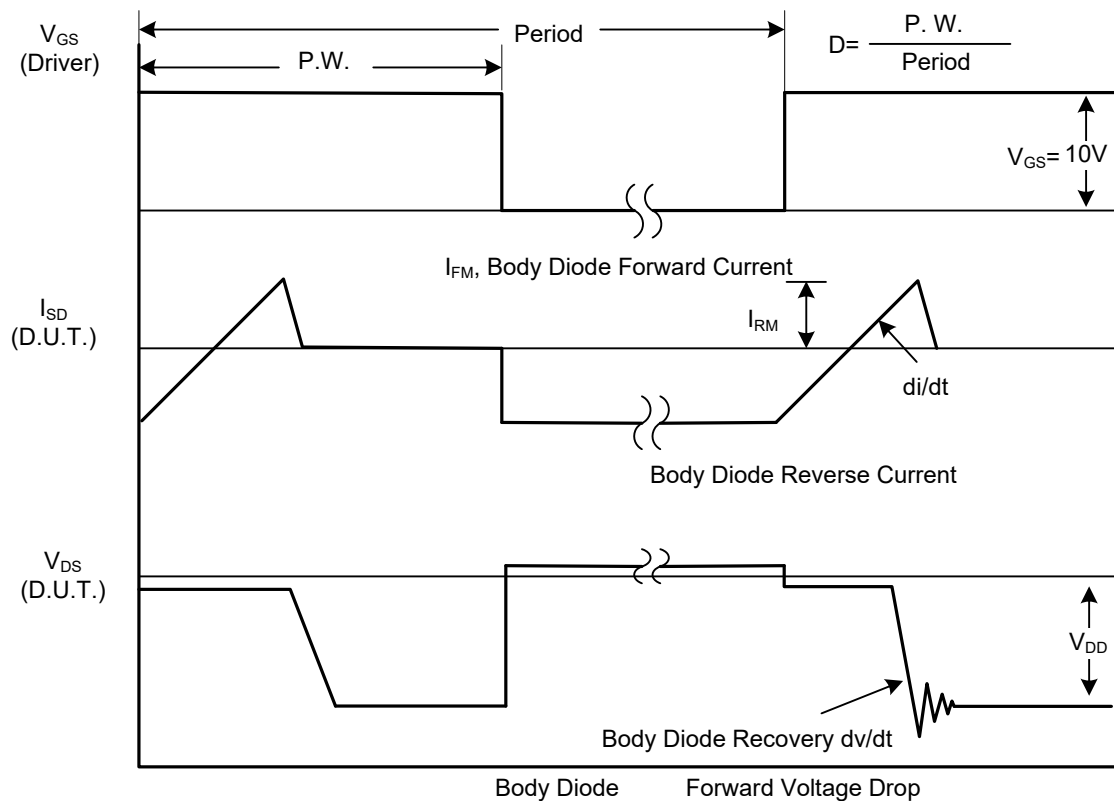
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

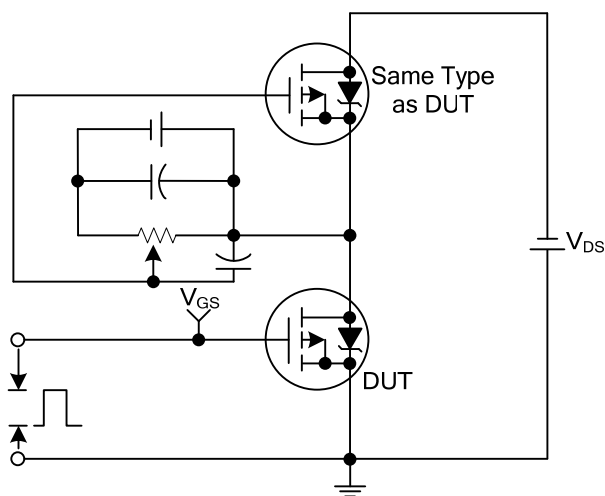


Peak Diode Recovery dv/dt Test Circuit

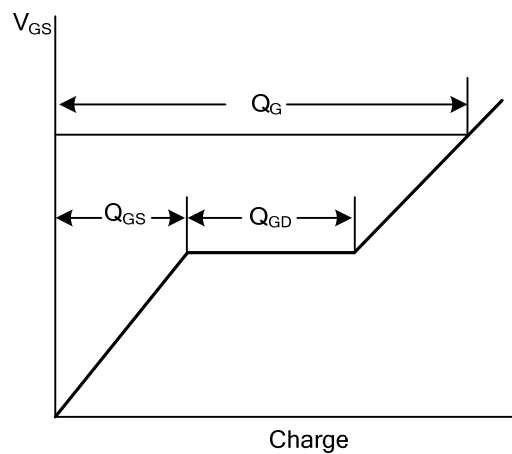


Peak Diode Recovery dv/dt Waveforms

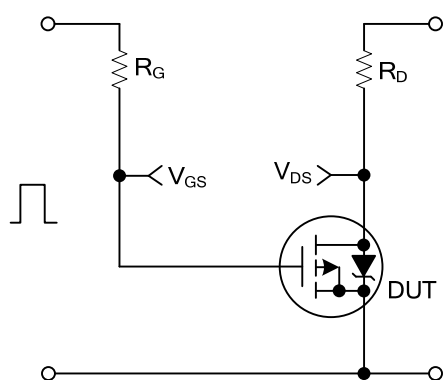
■ TEST CIRCUITS AND WAVEFORMS



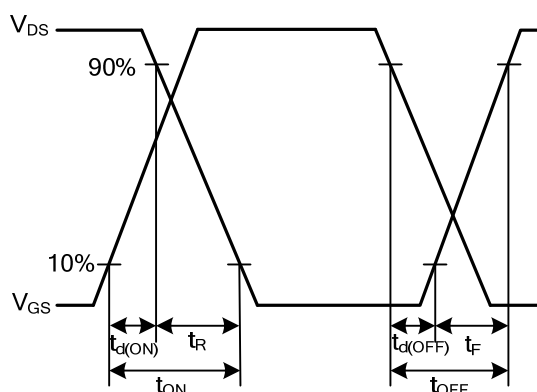
Gate Charge Test Circuit



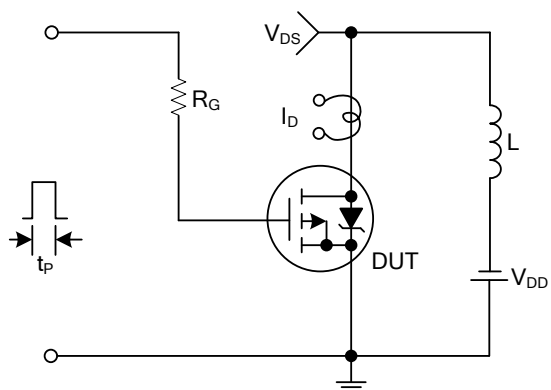
Gate Charge Waveforms



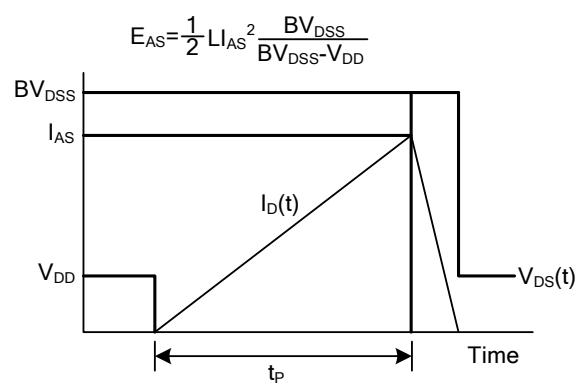
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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