

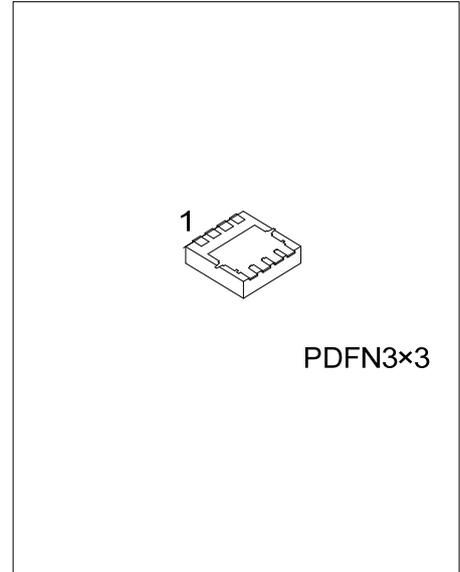


UT7430

Preliminary

Power MOSFET

30V, 34A N-CHANNEL ENHANCEMENT MODE POWER MOSFET



DESCRIPTION

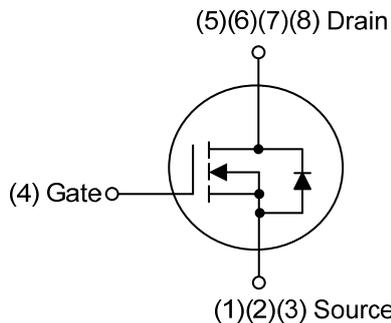
The UTC **UT7430** is an N-Channel MOSFET, it uses UTC's advanced technology to provide customers with a minimum on-state resistance, high switching speed and low gate charge.

The UTC **UT7430** is suitable for general purpose applications and high side switch in SMPS.

FEATURES

- * $R_{DS(ON)} \leq 12 \text{ m}\Omega @ V_{GS}=10V, I_D=20A$
- * $R_{DS(ON)} \leq 16 \text{ m}\Omega @ V_{GS}=4.5V, I_D=20A$
- * Low gate charge
- * High switching speed

SYMBOL



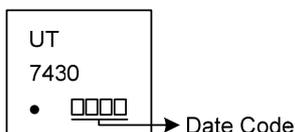
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment						Packing		
Lead Free	Halogen Free		1	2	3	4	5	6		7	8
UT7430L-P3030-R	UT7430G-P3030-R	PDFN3x3	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT7430G-P3030-R</p>	<p>(1) R: Tape Reel</p> <p>(2) P3030: PDFN3x3</p> <p>(3) G: Halogen Free and Lead Free, K: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		V_{DSS}	30	V	
Gate-Source Voltage		V_{GSS}	± 20	V	
Drain Current	Continuous	I_D	$T_C=25^\circ\text{C}$	34	A
			$T_C=100^\circ\text{C}$	21	A
	Pulsed (Note 3)		I_{DM}	80	A
Repetitive Avalanche Energy	$L=0.1\text{mH}$ (Note 3)		E_{AS}	25.5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	0.95	V/nS	
Power Dissipation (Note 2)		P_D	24	W	
Junction Temperature		T_J	-55 ~ +150	$^\circ\text{C}$	
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L = 0.1\text{mH}$, $I_{AS} = 22.6\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 34.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	75	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	5.2	$^\circ\text{C}/\text{W}$

Notes: 1. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

2. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

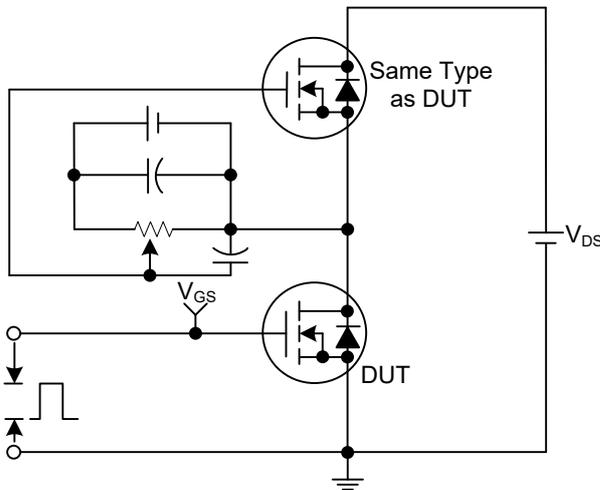
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

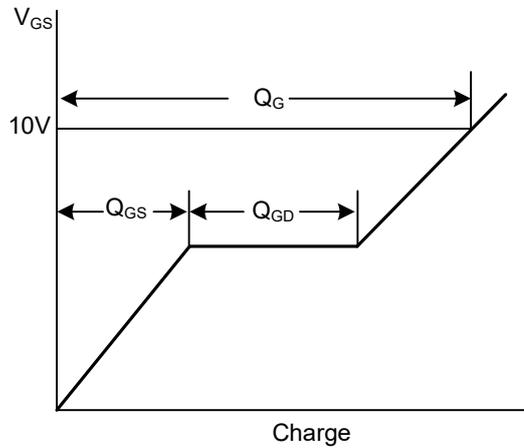
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	30			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	V _{GS} =+20V, V _{DS} =0V			100	nA
	Reverse	V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A			12	mΩ
		V _{GS} =4.5V, I _D =20A			16	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =15V, f=1.0MHz		718		pF
Output Capacitance	C _{OSS}			199		pF
Reverse Transfer Capacitance	C _{RSS}			168		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =24V, V _{GS} =10V, I _D =34A		14		nC
Gate to Source Charge	Q _{GS}			3		nC
Gate to Drain Charge	Q _{GD}			9		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DS} =15V, V _{GS} =10V, I _D =34A R _G =3Ω		7		ns
Rise Time	t _R			16		ns
Turn-OFF Delay Time	t _{D(OFF)}			18		ns
Fall-Time	t _F			20		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				34	A
Maximum Body-Diode Pulsed Current	I _{SM}				80	A
Drain-Source Diode Forward Voltage	V _{SD}	I _S =1.0A, V _{GS} =0V			1.0	V
Reverse Recovery Time (Note 1)	t _{rr}	I _S =30A, V _{GS} =0V, dI/dt=100A/μs		210		nS
Reverse Recovery Charge	Q _{rr}			353		nC

Notes: 1. Pulse Test: Pulse width ≤ 1200μs, Duty cycle ≤ 2%.
 2. Essentially independent of operating temperature.

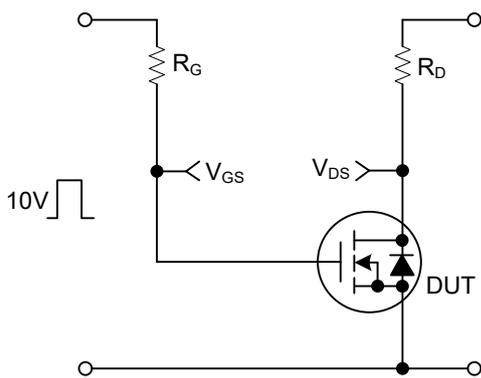
■ TEST CIRCUITS AND WAVEFORMS



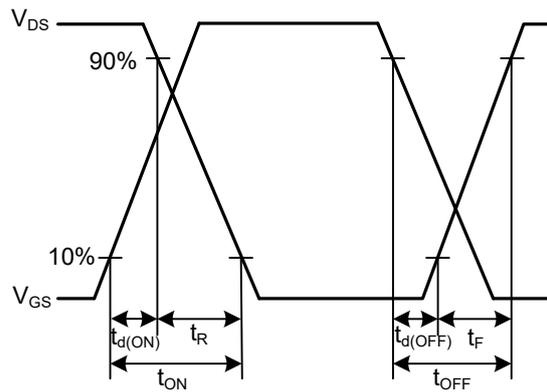
Gate Charge Test Circuit



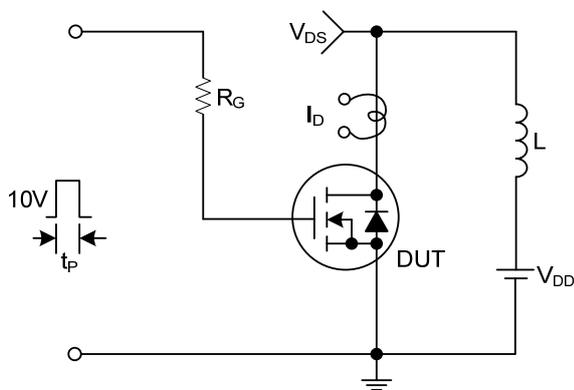
Gate Charge Waveforms



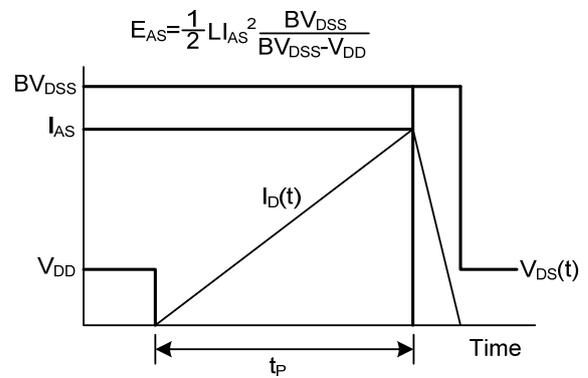
Resistive Switching Test Circuit



Resistive Switching Waveforms

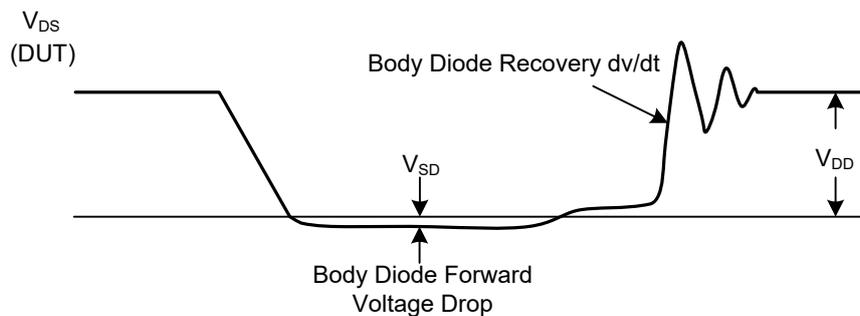
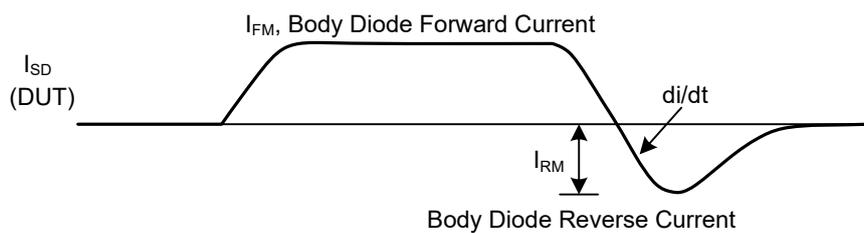
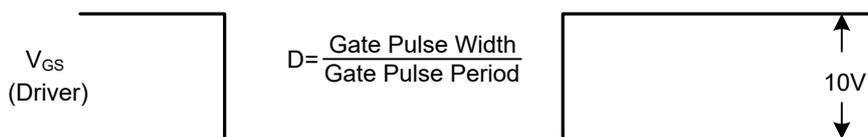
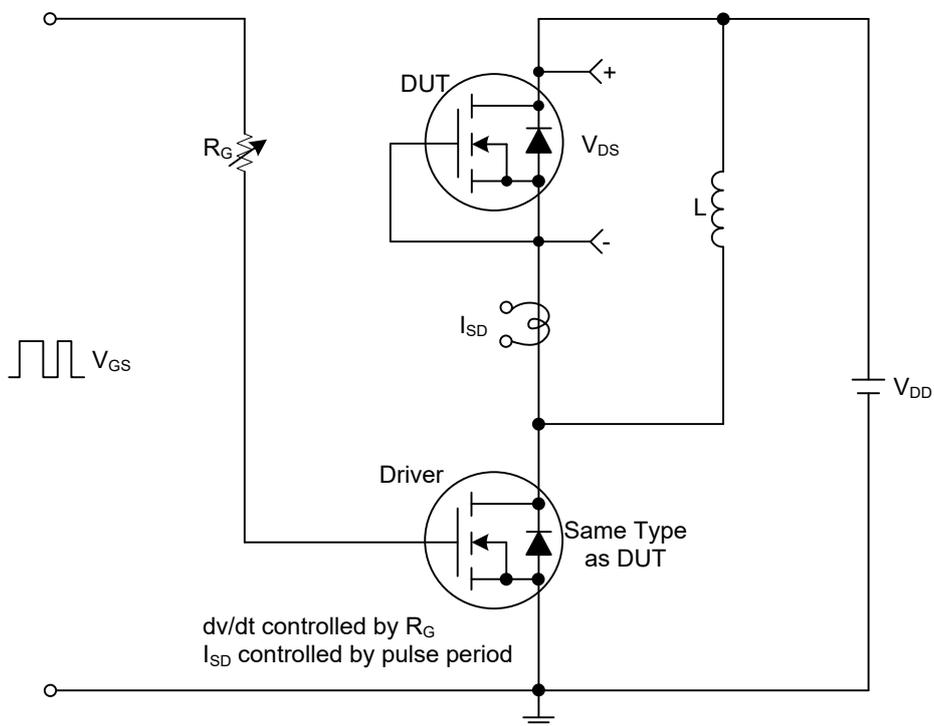


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS



Peak Diode Recovery dv/dt Test Circuit and Waveforms

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