



UT85P03

Preliminary

POWER MOSFET

-85A, -30V P-CHANNEL ENHANCEMENT MODE POWER MOSFET

DESCRIPTION

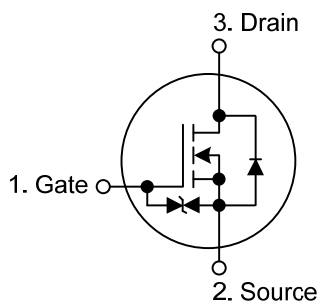
The UTC **UT85P03** is P-Channel enhancement mode Power MOSFET, designed in serried ranks with fast switching speed, low on-resistance and favorable stabilization.

Used in commercial and industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

FEATURES

- * $R_{DS(ON)} \leq 7.2 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$, $I_D = -42.5\text{A}$
 $R_{DS(ON)} \leq 9.8 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -42.5\text{A}$
- * Low Capacitance
- * Optimized gate charge
- * Fast switching capability
- * Avalanche energy specified

SYMBOL

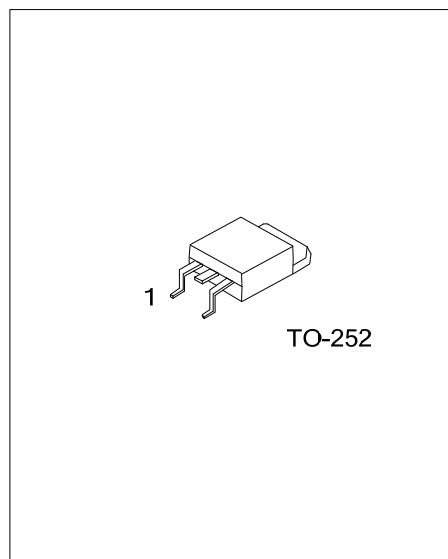


ORDERING INFORMATION

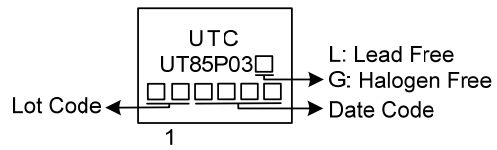
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT85P03L-TN3-R	UT85P03G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT85P03G-TN3-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) TN3: TO-252
		(3) Green Package	(3) G: Halogen Free and Lead Free L: Lead Free



■ MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	DC	I_D	-85	A
	Pulsed (Note 2)	I_{DM}	-170	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	151	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	0.3	V/ns
Power Dissipation		P_D	54	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS} = -55.1\text{A}$, $V_{DD}=-50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$.

4. $I_{SD} \leq -30.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^{\circ}\text{C}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.3 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

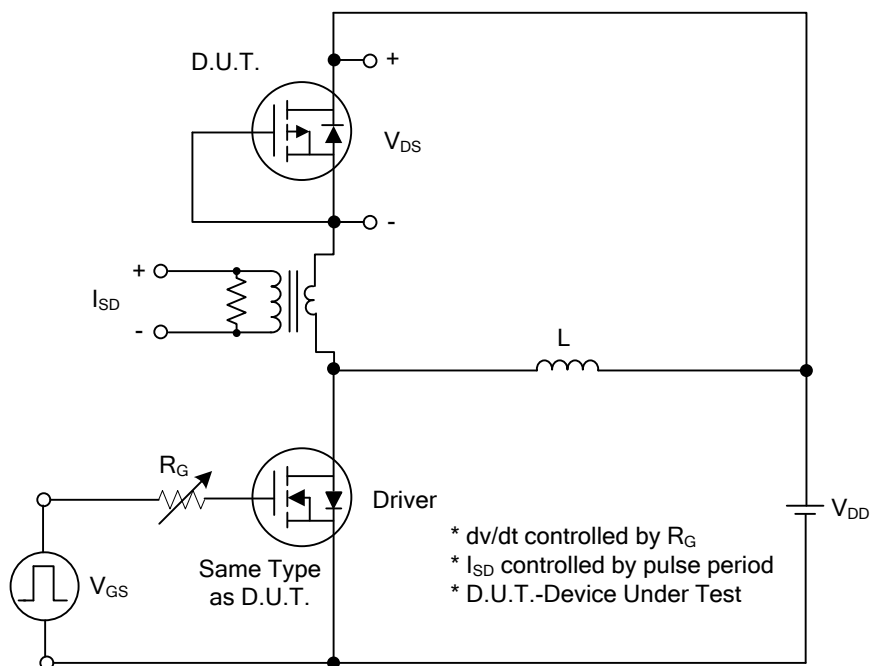
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-30			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V			-1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance (Note)	R _{DS(ON)}	V _{GS} =-10V, I _D =-42.5A			7.2	mΩ
		V _{GS} =-4.5V, I _D =-42.5A			9.8	mΩ
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{DS} =-25V, V _{GS} =0V, f=1.0MHz		5180		pF
Output Capacitance	C _{OSS}			805		pF
Reverse Transfer Capacitance	C _{RSS}			680		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q _G	V _{DS} =-24V, V _{GS} =-10V, I _D =-85A (Note 1, 2)		105		nC
Gate-Source Charge	Q _{GS}			13		nC
Gate-Drain Charge	Q _{GD}			30		nC
Turn-On Delay Time	t _{D(ON)}	V _{DS} =-15V, V _{GS} =-10V, I _D =-85A, R _G =3Ω (Note 1, 2)		14		ns
Turn-On Rise Time	t _R			18		ns
Turn-Off Delay Time	t _{D(OFF)}			240		ns
Turn-Off Fall Time	t _F			140		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				-85	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				-170	A
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =-85A			-1.2	V
Body Diode Reverse Recovery Time	t _{RR}	I _F =-30A, di/dt=100A/μs		204		ns
Body Diode Reverse Recovery Charge	Q _{RR}			0.7		us

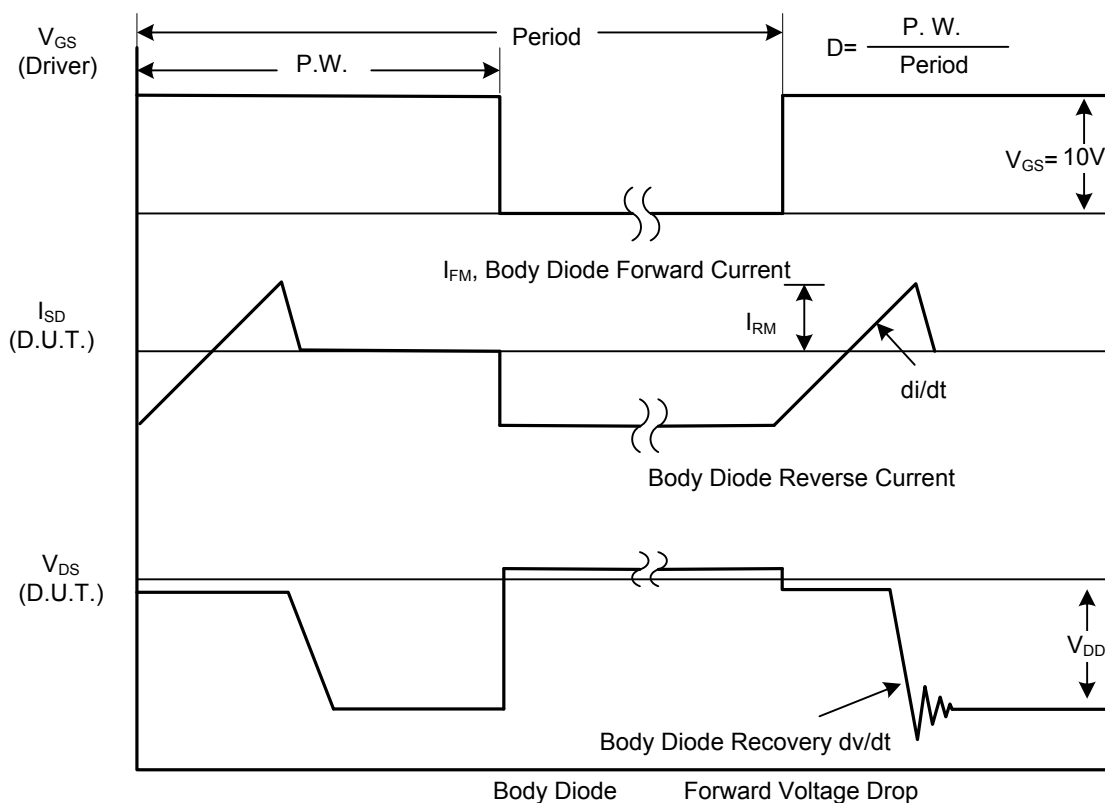
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

TEST CIRCUITS AND WAVEFORMS

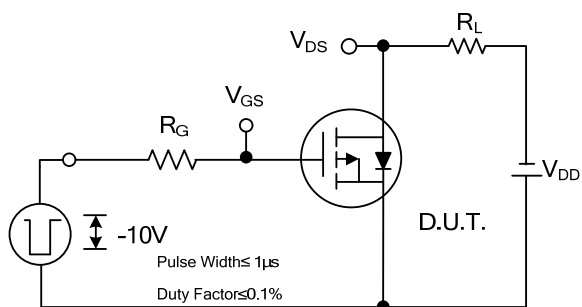


Peak Diode Recovery dv/dt Test Circuit

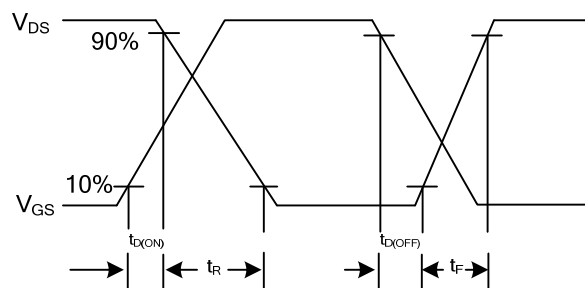


Peak Diode Recovery dv/dt Waveforms

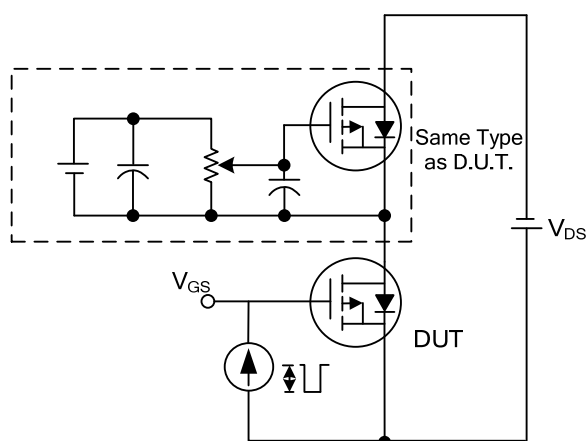
■ TEST CIRCUITS AND WAVEFORMS



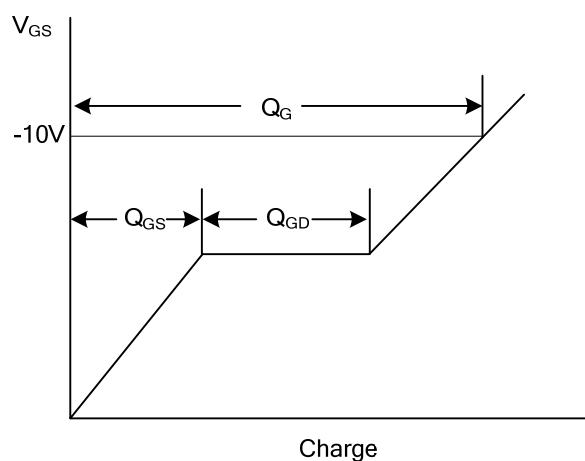
Switching Test Circuit



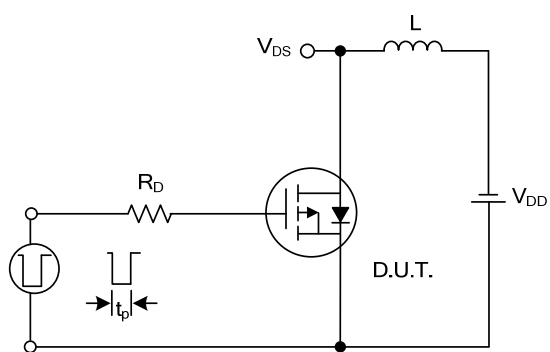
Switching Waveforms



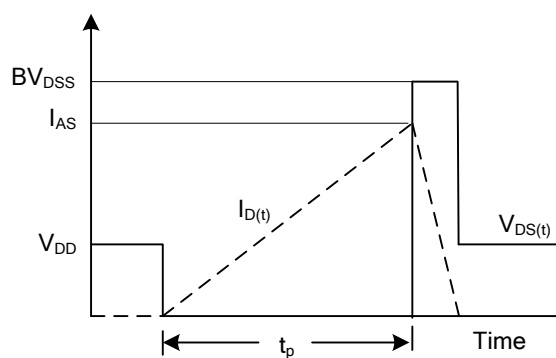
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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