

**UT9Z24**

Preliminary

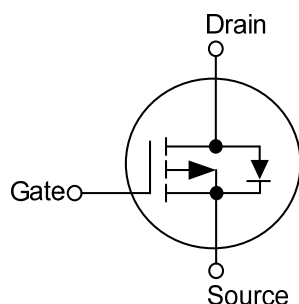
Power MOSFET

**-17A, -55V P-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **UT9Z24** is a P-channel enhancement mode power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance. The UTC **UT9Z24** is suitable for high efficiency synchronous rectification in SMPS, primary side switch and telecom bricks.

FEATURES

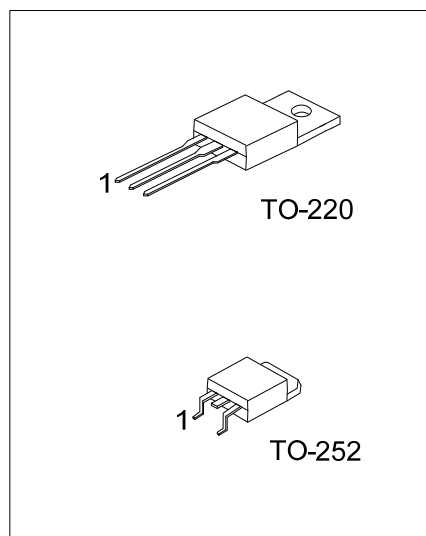
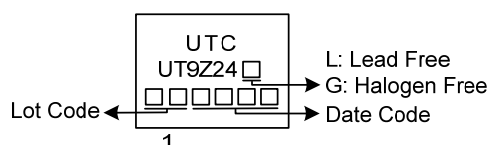
- * $R_{DS(ON)} \leq 58 \text{ m}\Omega$ @ $V_{GS} = -10\text{V}$, $I_D = -10\text{A}$
- $R_{DS(ON)} \leq 90 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -10\text{A}$
- * High switching speed
- * Low gate charge

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT9Z24L-TA3-T	UT9Z24G-TA3-T	TO-220	G	D	S	Tube
UT9Z24L-TN3-R	UT9Z24G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

		(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TN3: TO-252 (3) G: Halogen Free and Lead Free L: Lead Free
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MARKING

■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	-55	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	-17	A
	Pulsed	I_{DM}	-34	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	43	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	9	V/ns
Power Dissipation	TO-220	P_D	100	W
	TO-252		48	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{AS}=-29\text{A}$, $V_{DD}=-25\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq -9.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
	TO-252		50	$^{\circ}\text{C}/\text{W}$
Junction to Case	TO-220	θ_{JC}	1.25	$^{\circ}\text{C}/\text{W}$
	TO-252		2.6 (Note)	$^{\circ}\text{C}/\text{W}$

Note: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

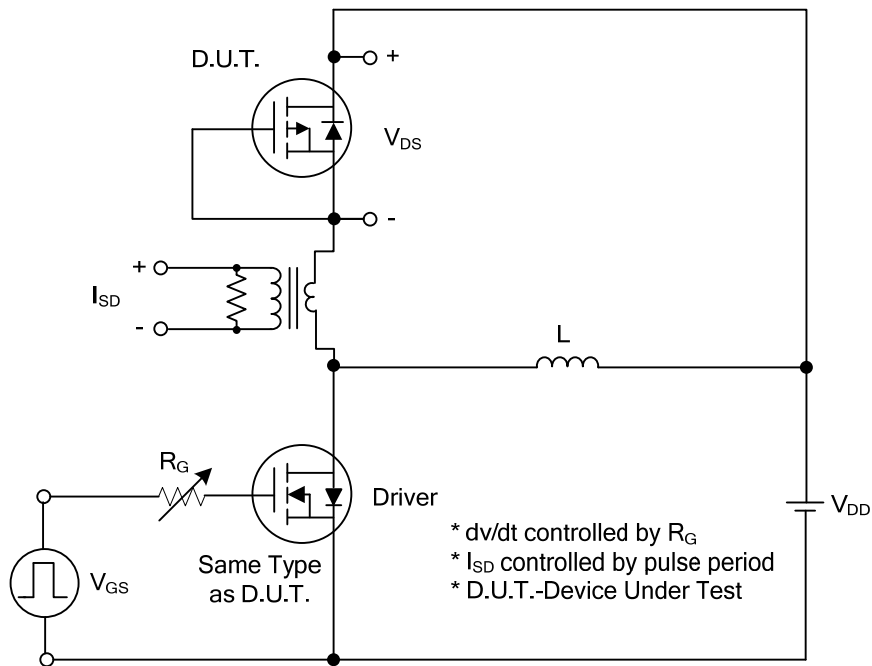
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =-250μA, V _{GS} =0V	-55			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-55V, V _{GS} =0V			-1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-10A			58	mΩ
		V _{GS} =-4.5V, I _D =-10A			90	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz		1370		pF
Output Capacitance	C _{OSS}			125		pF
Reverse Transfer Capacitance	C _{RSS}			80		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =-44V, V _{GS} =-10V, I _D =-9.0A (Note 1, 2)		30		nC
Gate to Source Charge	Q _{GS}			7		nC
Gate to Drain Charge	Q _{GD}			6		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =-30V, V _{GS} =-10V, I _D =-9.0A, R _G =3.3Ω (Note 1, 2)		7		ns
Turn-ON Rise Time	t _R			18		ns
Turn-OFF Delay Time	t _{D(OFF)}			37		ns
Turn-OFF Fall-Time	t _F			20		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				-17	A
Maximum Body-Diode Pulsed Current	I _{SM}				-34	A
Diode Forward Voltage	V _{SD}	I _S =-9.0A, V _{GS} =0V			-1.4	V
Body Diode Reverse Recovery Time (Note 1)	t _{rr}	I _S =-9.0A, V _{GS} =0V dI _F /dt=100A/μs		35		nS
Body Diode Reverse Recovery Charge	Q _{rr}			32		nC

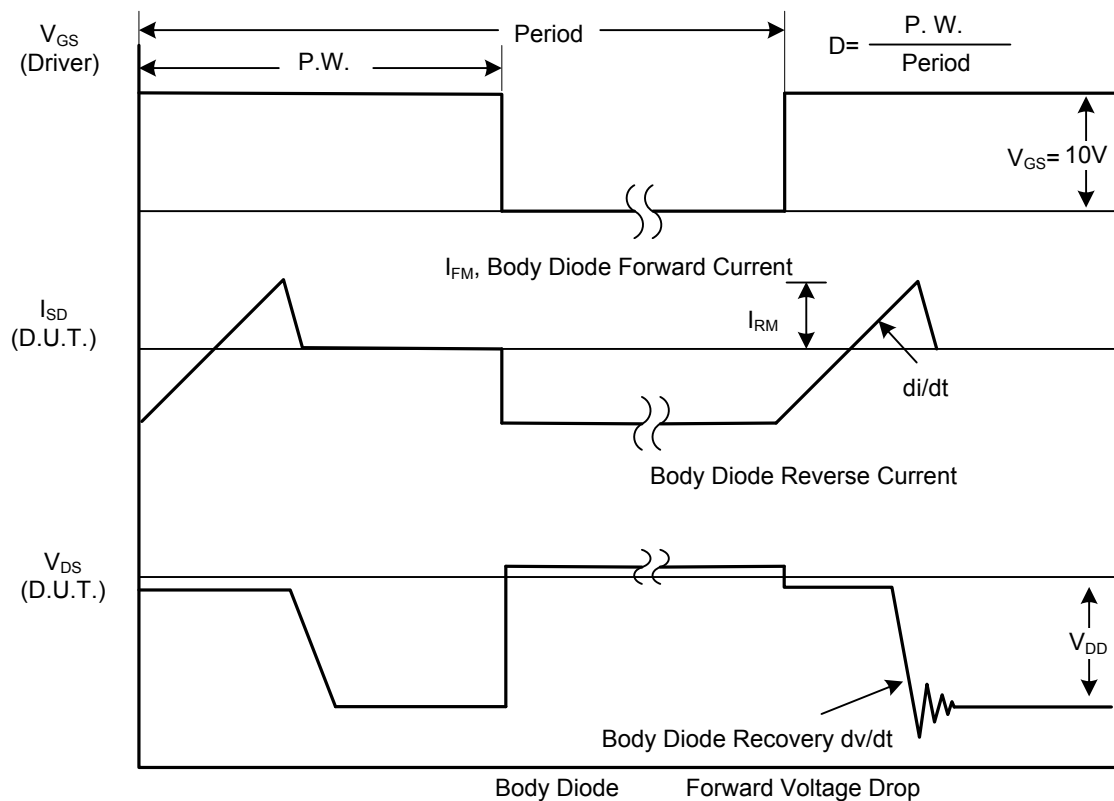
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

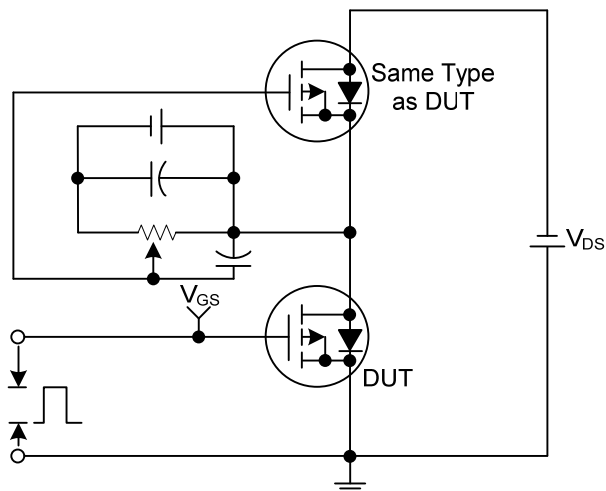


Peak Diode Recovery dv/dt Test Circuit

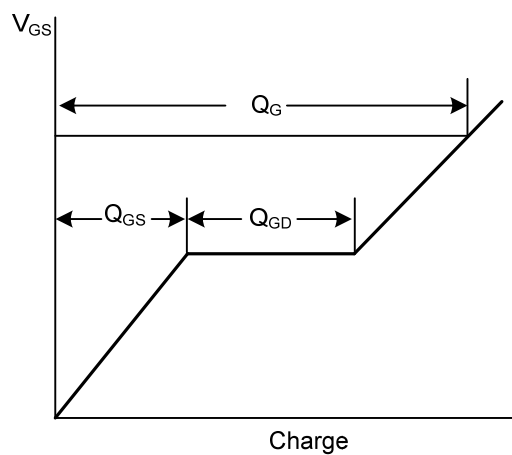


Peak Diode Recovery dv/dt Waveforms

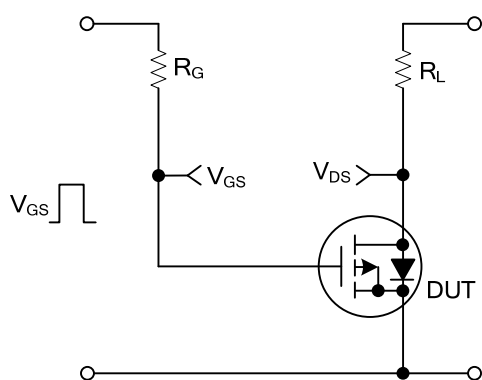
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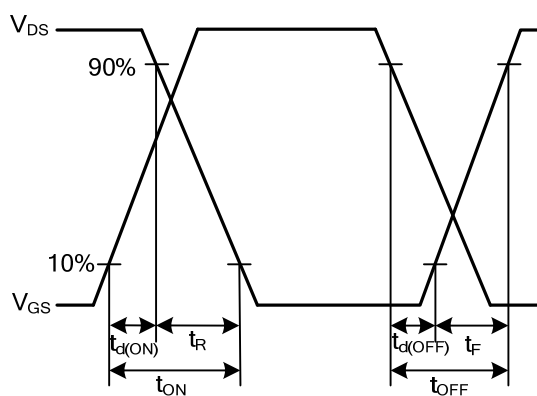
Gate Charge Test Circuit



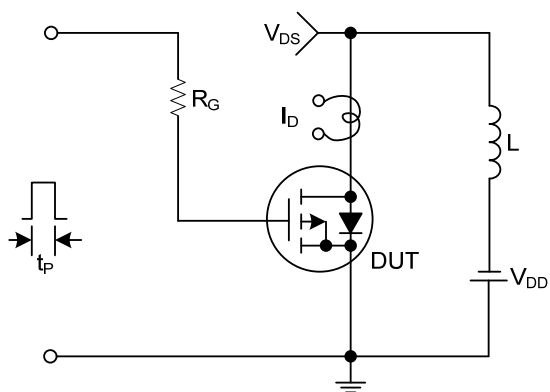
Gate Charge Waveforms



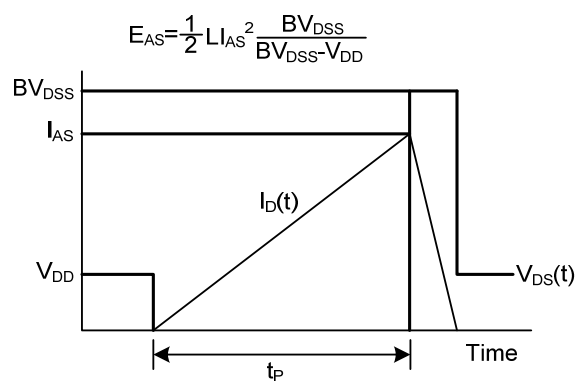
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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