



UTT25N04

POWER MOSFET

25A, 40V N-CHANNEL POWER MOSFET

DESCRIPTION

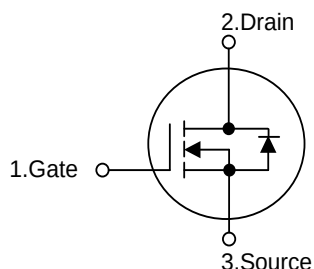
The UTC **UTT25N04** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance, low gate charge and high switching speed.

The UTC **UTT25N04** is suitable for high voltage synchronous rectifier and DC/DC converters, etc.

FEATURES

- * $R_{DS(ON)} \leq 28 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=12.5\text{A}$
- $R_{DS(ON)} \leq 52 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=12.5\text{A}$
- * High Switching Speed
- * High Cell Density Trench Technology

SYMBOL



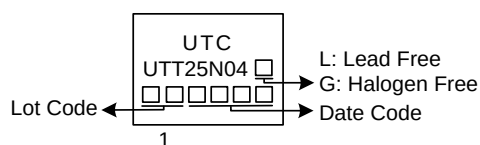
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT25N04L-TN3-R	UTT25N04G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT25N04G-TN3-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ ABSOLUTE MAXIMUM RATING ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current ($T_C = 25^\circ\text{C}$)	Continuous	I_D	25	A
	Pulsed (Note 2)	I_{DM}	50	A
Avalanche Energy (Note 3)	Single Pulsed (Note 3)	E_{AS}	22	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	25	V/nS
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	28	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. $L = 0.1\text{mH}$, $I_{AS} = 21\text{A}$, $V_{DD} = 25\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 25\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	4.46 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

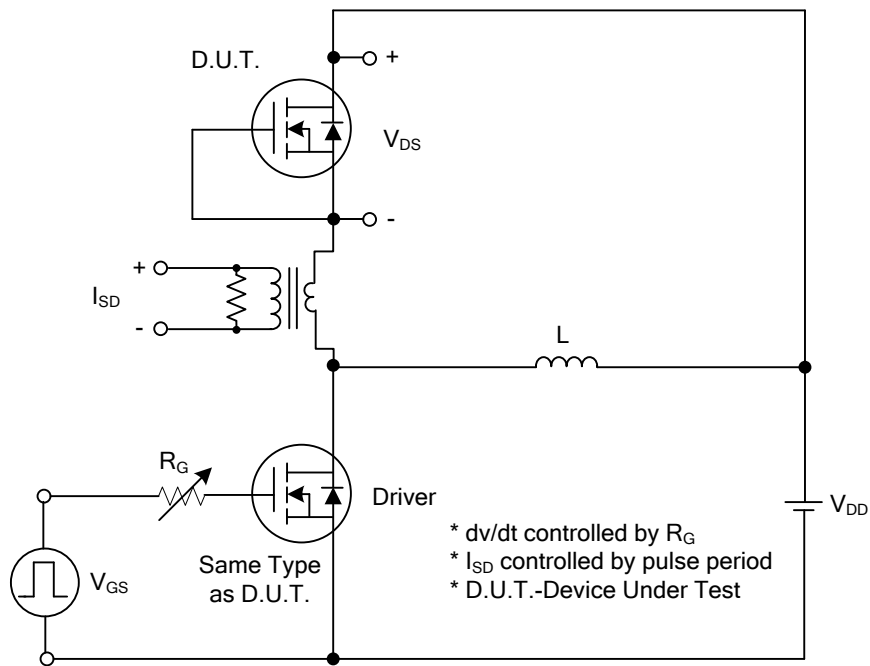
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+5	μA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-5	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =12.5A			28	mΩ
			V _{GS} =4.5V, I _D =12.5A			52	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		570		pF
Output Capacitance		C _{OSS}			90		pF
Reverse Transfer Capacitance		C _{RSS}			70		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =40V, V _{GS} =10V, I _D =25A I _G =1mA (Note 1, 2)		19		nC
Gate to Source Charge		Q _{GS}			2.1		nC
Gate to Drain Charge		Q _{GD}			5		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DS} =40V, V _{GS} =10V, I _D =25A, R _G =25Ω (Note 1, 2)		4		ns
Rise Time		t _R			21		ns
Turn-off Delay Time		t _{D(OFF)}			76		ns
Fall-Time		t _F			49		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				25	A
Maximum Body-Diode Pulsed Current		I _{SM}				50	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =25A, V _{GS} =0V			1.4	V
Reverse Recovery Time (Note 1)		t _{rr}	I _S =25A, V _{GS} =0V,		40		nS
Reverse Recovery Charge		Q _{rr}	dl/dt=100A/μs		18		nC

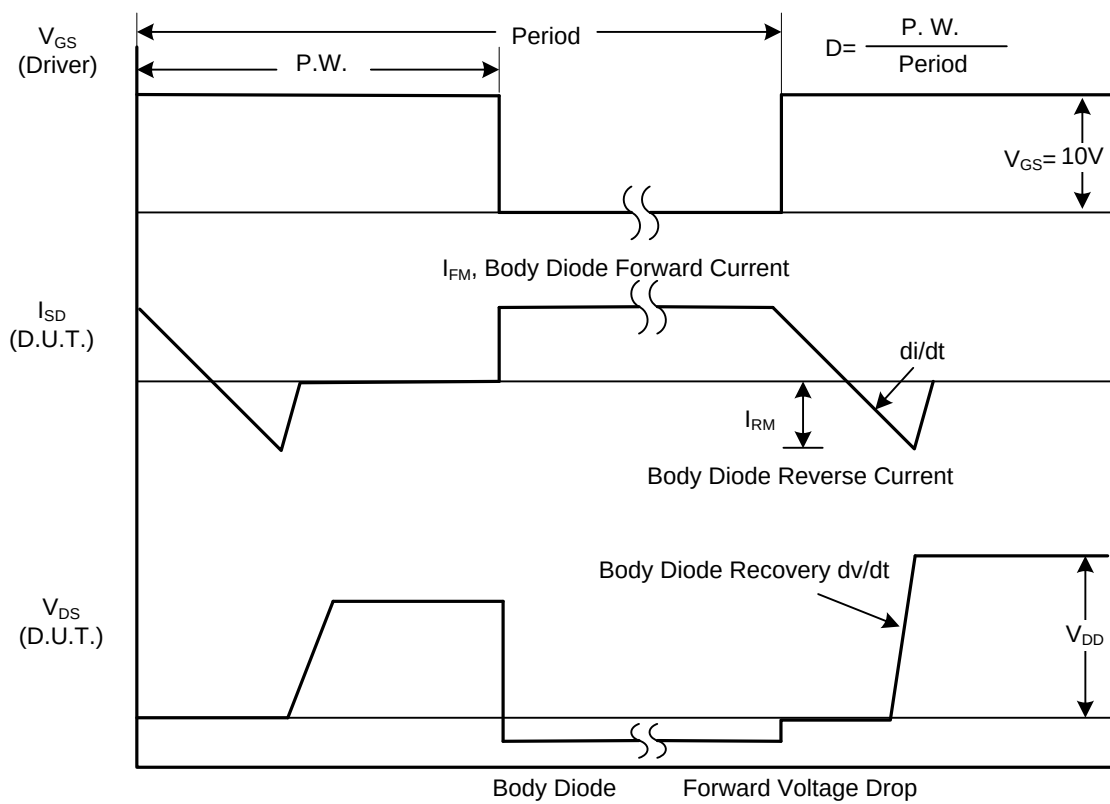
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

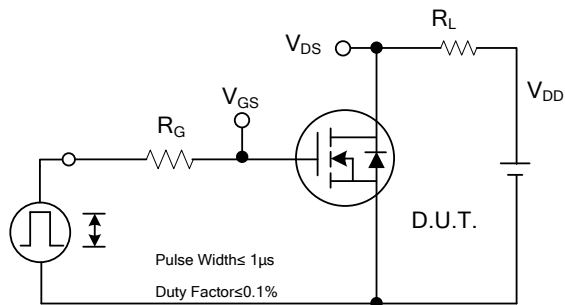


Peak Diode Recovery dv/dt Test Circuit

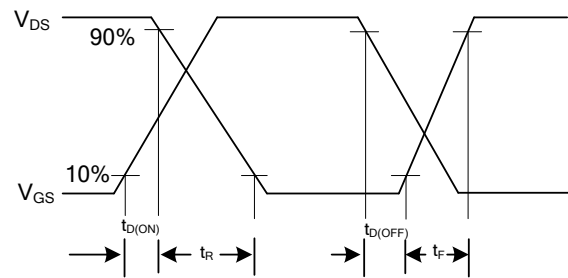


Peak Diode Recovery dv/dt Waveforms

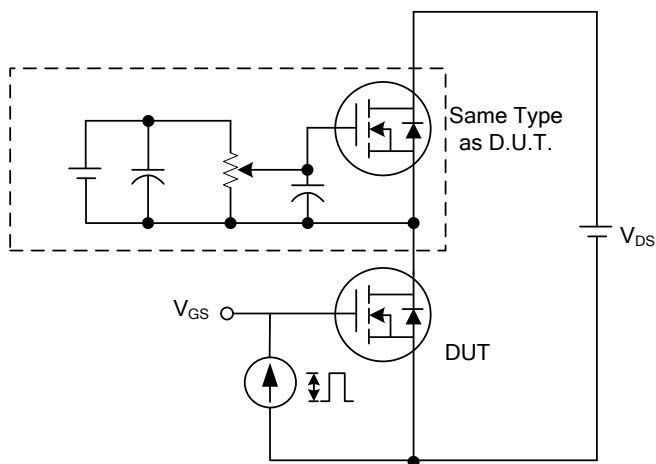
■ TEST CIRCUITS AND WAVEFORMS



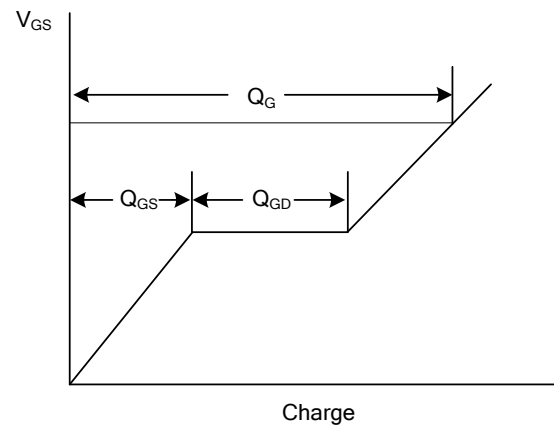
Switching Test Circuit



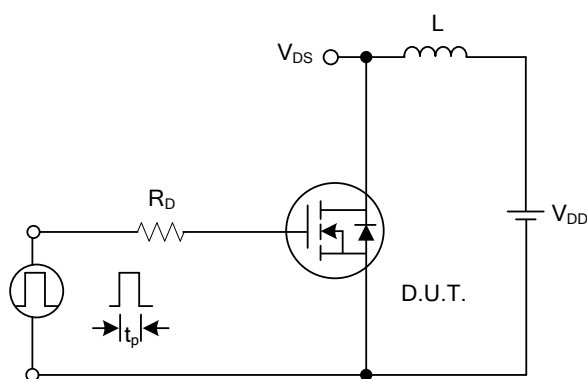
Switching Waveforms



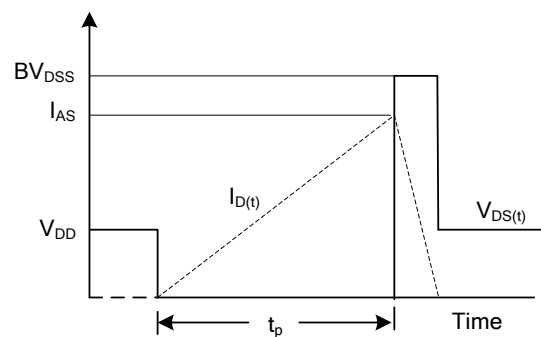
Gate Charge Test Circuit



Gate Charge Waveform

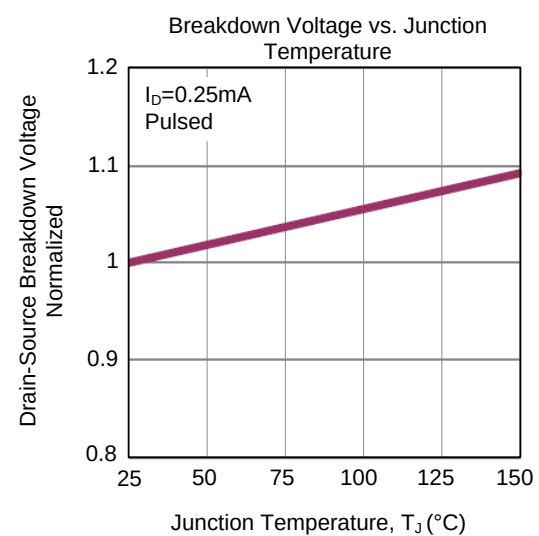
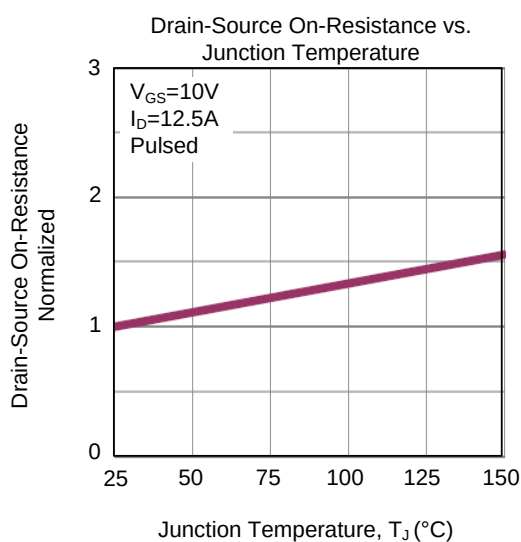
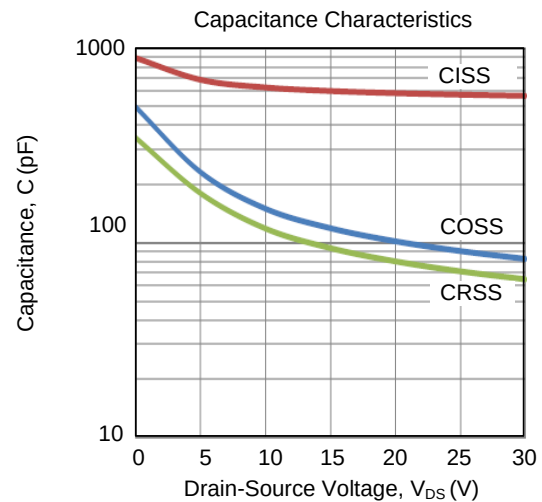
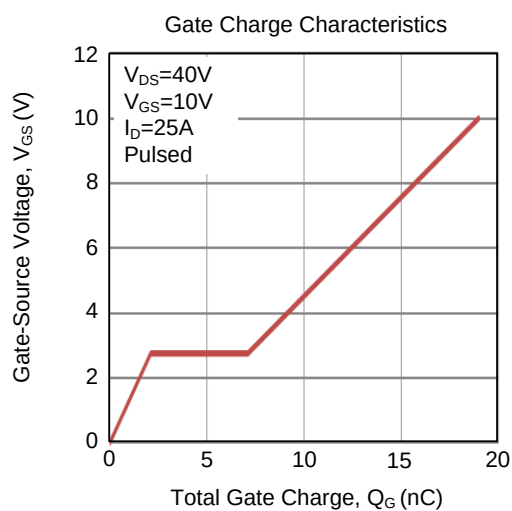
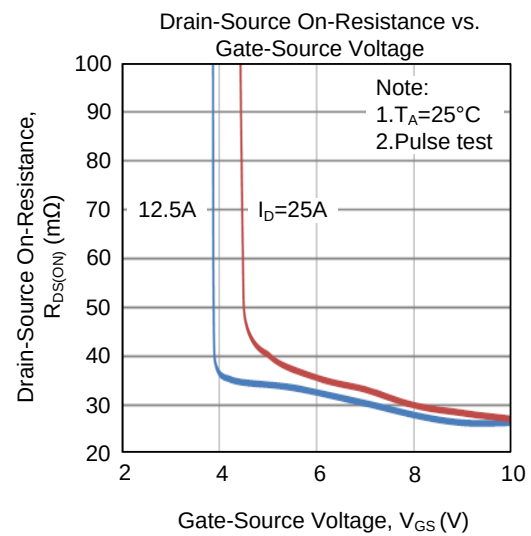
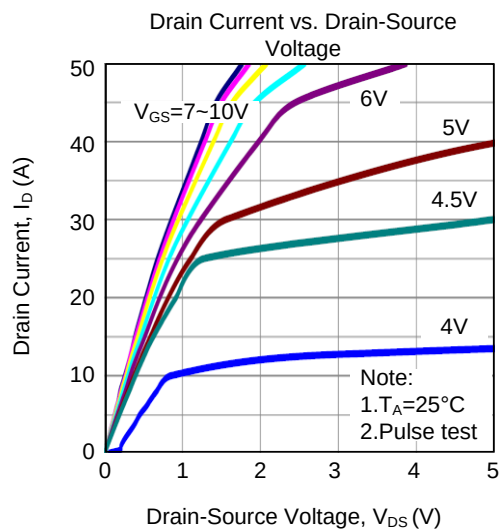


Unclamped Inductive Switching Test Circuit

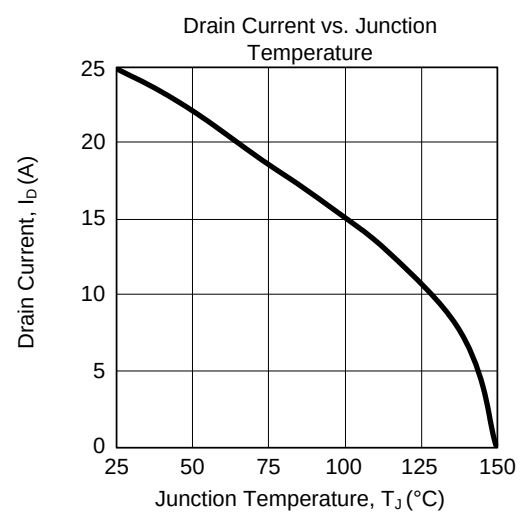
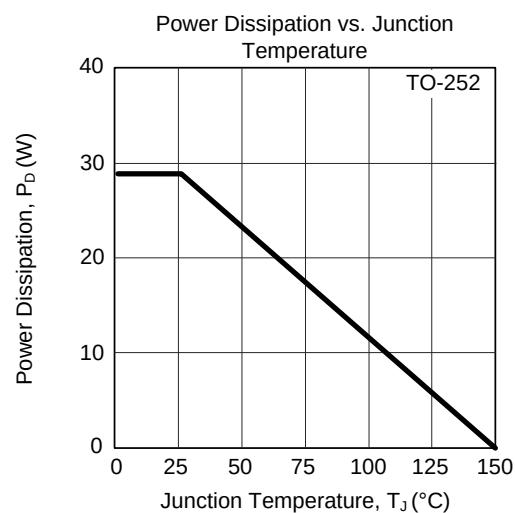
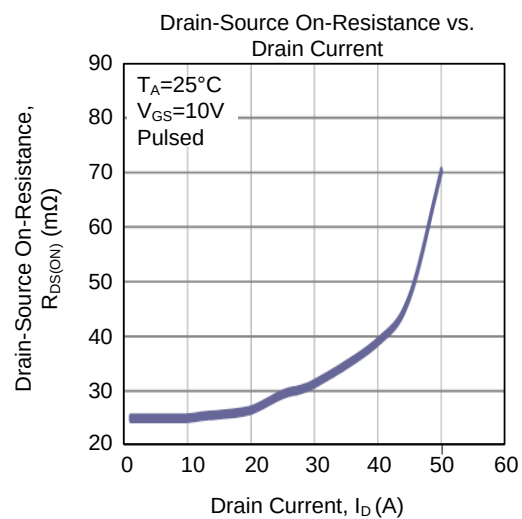
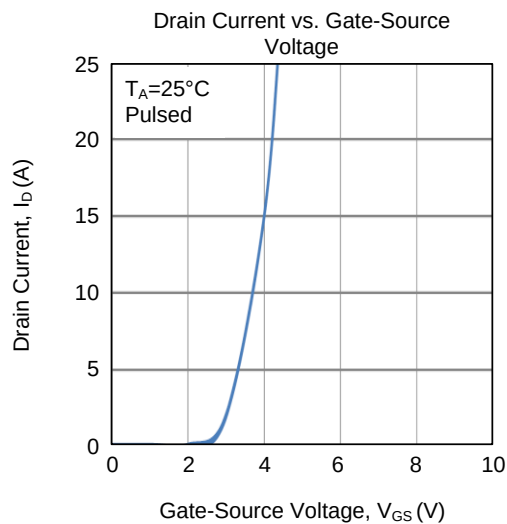
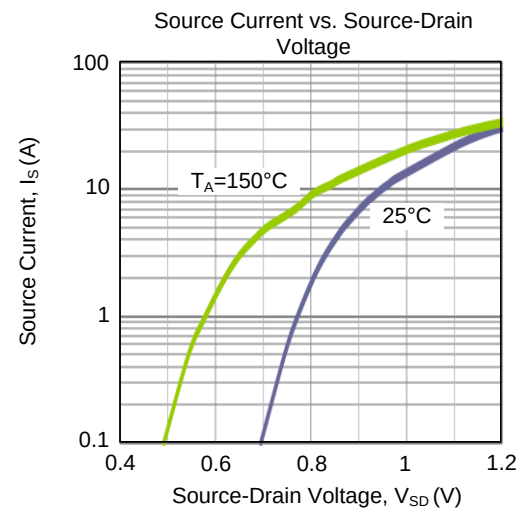
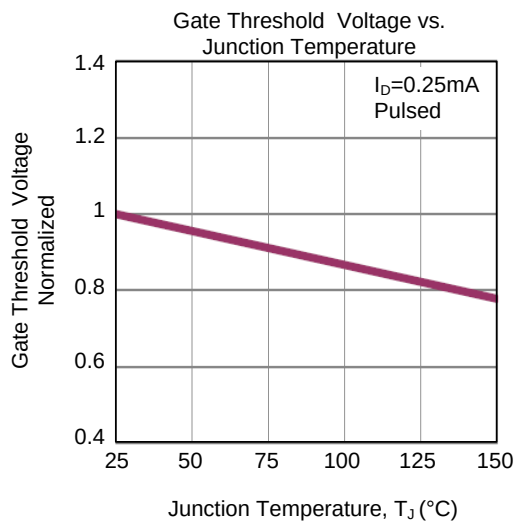


Unclamped Inductive Switching Waveforms

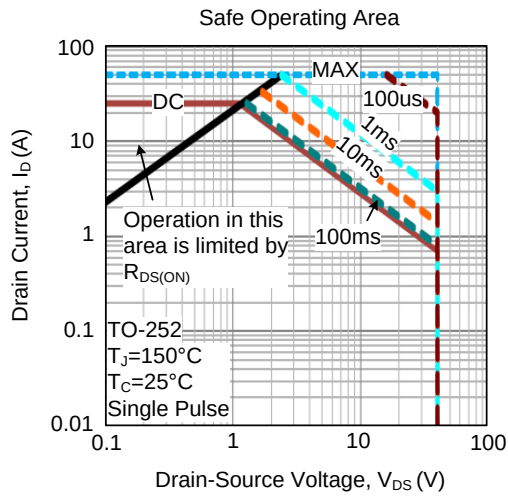
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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